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Modeling and design of matching-critical circuits

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Modeling and design of matching-critical circuits

by

Mao-Feng Lan

A dissertation submitted to the graduate faculty

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This is to certify that the Doctoral dissertation of

Mao-Feng Lan

has met the dissertation requirements of Iowa State University

Signature was redacted for privacy.

Major Professor

Signature was redacted for privacy.

For the Major Program

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For the Graduate College

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ABSTRACT

Existing approaches for modeling mismatch effects in matching-critical circuits are based upon models derived under the widely accepted premise that distributed parameter devices can be modeled with lumped parameter models. It is shown in this dissertation that the lumped parameter models do not consistently reflect device performance and introduce substantial errors in matching-critical circuits if either systematic or random parameter variations occur in the channel. A new approach for characterizing the effects of both systematic and random variations in semiconductor device properties on device matching is introduced. This approach circumvents the introduction of model errors inherent in the existing approaches. A CAD tool, MOSGRAD, was developed to simulate the effects of distributed two-dimensional systematic and random variations in device parameters on the performance of matching-critical circuits. The tool is capable of predicting the performance of non-conventional circuit structures in which multiple drain and/or source regions that may or may not be rectangular and/or multiply segmented. Through the use of the tool, new current mirror layout strategies have been developed that exhibit reduced sensitivity to matching in the presence of linear parameter gradients.

CHAPTER 1. GENERAL INTRODUCTION

I. Introduction

The sophistication of data, image, and voice processing systems has been steadily increasing. As a result, the performances of requirements of the underlying analog circuits in these systems have also been increasing. Invariably these analog systems require close matching of current sources, precise control of current mirror gains, and/or very low input referred offset voltages in differential amplifiers. It is well known that the performance of these circuits depend on how closely the I/V characteristics of two transistors can be matched. The shrinkage of feature sizes and the reduction of supply voltages generally degrade matching performance. In most of the published matching research [1-4], the matching characteristics are attributed to systematic and random variations in both geometric parameters and process parameters. It has been reported and is widely accepted that the mismatch due to random parameter variations is inversely proportional to the active area of the matching critical transistors and thus, tradeoffs can be made between area and performance to compensate for random variations. It is also widely accepted that the systematic variations can be modeled as stochastic processes with long correlation distances that can be reduced or eliminated by placing the matching-critical transistors close to one another using a segmented common centroid layout technique. With the existing approaches to predicting matching characteristics, considerable discrepancies between predicted performance and actual measured performance exist. These discrepancies are inherently attributable to limitations of the models used to predict the matching performance. In this work, consistency and limitations of existing models and their impact on predicting the

performances of analog circuits will be discussed. A new stochastic model is presented that offers improvement in predicting the effects of random parameter variations on device matching. A new CAD tool, MOSGRAD, capable of modeling lateral parameter variations has been developed. This tool can be used to accurately predict the effects of systematic and random parameter variations on the performance of current mirrors. With the help of MOSGRAD, new layout techniques that have improved matching characteristics over what is achievable with the common centroid technique have been proposed and simulated.

II. Contributions

This work focuses on the modeling and design of matching-critical circuits. The main objective is to produce a more accurate method for modeling matching performance. The application of this research will provide engineers valuable insight into matching performance and its limitations. The newly developed CAD tool is useful for investigating the matching performance of alternative layout structures. Its use may lead to the discovery of new layout techniques that have superior matching performance to the layout techniques commonly used today. The contributions of this dissertation can generally be subdivided into 4 parts.

A. Investigation of the Limitations of the Integral Model

Essentially all device models and, in particular, the device models used in Spice-based simulators are based upon lumped parameter models. In [1-4], it is assumed that the actual values of the lumped model parameters can be obtained by integrating the position-

dependent distributed model parameters over the area of the channel region of the device as given by the equation.

$$\gamma(x_A, y_A) = \frac{1}{\text{Area}} \iint_{\text{Area}} \gamma(x, y)\,dxdy \qquad (1)$$

where (x_A,y_A) is a point representation of the location of the device on the die. Although not critical, it is convenient to define (x_A,y_A) to be the geometrical center of the device. This lumped parameter extraction from a distributed parameter domain is referred to the integral model. The approach of mapping from a distributed stochastic parameter to a single lumped model parameter has been used almost exclusively for well over a decade and its validity has not been questioned. Since both systematic effects and random fluctuations in device parameters are known to play important roles in matching performance, it is particularly important that the lumped device models effectively incorporate these effects. The failure to incorporate these fluctuations is pointed out in this dissertation and the effects of the integral model on the predictions of systematic and random variations will be investigated and discussed.

B. Consistent Random Parameter Variation Model

It is well recognized that the random parameter variation is inversely proportional to the active area and can be expressed as

$$\sigma^2(\gamma) = \frac{A_\gamma^2}{\text{Area}} \qquad (2)$$

where γ can be a model or process parameter and A_γ is an area proportionality constant [3].

When $\sigma(\gamma)$ is plotted as a function of $1/\sqrt{Area}$, A_γ will be the slope of the curve [3]. $\sigma(\gamma)$ is extracted from the measurement of I/V characteristics and the extraction formula used in the triode region can be expressed as

$$I_D = \beta \frac{(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}}{1 + \theta (V_{GS} - V_T)} \tag{3}$$

where $\beta=C_{OX}\mu W/L$ is the current factor and θ the mobility degradation coefficient [3]. γ can be the threshold voltage (V_{T0}), the mobility (μ), and the gate oxide capacitance density (Cox), etc. Because the extracted A_γ will be used to represent the variation characteristics of the process, it should be independent of the shapes of devices. However, [5] shows a significant difference in A_γ's measured with hexagonal and rectangular transistors. This observation signals that the extracted value does not truly represent the inherent variation characteristics of the process. This discrepancy is mainly due to the fact that the extraction process was based upon lumped models derived using the integral model. It will also be shown that there is a consistency problem involving A_γ in this dissertation. Thus we propose an alternative approach for retrieving the model of random parameter variation that is based on a distributed domain viewpoint. It will be shown that the new model is consistent and it explains some unexpected observations on random variation measurements.

C. Simulation Tool for Predicting Matching Performance of Matching-Critical Circuits

The preferred route for optimizing the design and layout is based upon simulation. The seemingly simple problem of predicting the effects of systematic and random variations on a MOS transistor is not possible because a available. Existing models and simulators

provide little insight into how to change either the size or layout to improve matching performance. Existing simulators have no mechanism for incorporating either systematic or random channel variations in device dimensions or process parameters. These variations play a key role in the determining the matching performance of high-end circuits.

A simulation tool named MOSGRAD that can be used to simulate the effects of two-dimensional systematic and random variations in both process and device parameters on the performance of matching-critical circuits has been developed. With this tool, systematic variations in process or device parameters of any magnitude and at any angle relative to the cell can be simulated using a conventional SPICE-type simulator. Random variations can be simulated using MATLAB with the consistent random parameter variation model. The tool has been used to predict the effects of systematic and random parameter variations on the performance of several different current mirror layout structures. It has also been used to predict the performance of non-conventional circuit structures that may incorporate nonrectangular transistors or multiply-segmented transistors. It has successfully uncovered some fundamental limitations in the previously unquestioned relationship between the effects of random variations on circuit performance and gate area.

D. New Layout Techniques with reduced Sensitivity to Parameter Gradients

Several new common-centroid layout techniques that exhibit improved matching performance are introduced. One uses an interconnection of two 4-segment rectangular transistors. The others are non-rectangular structures in which the active region is continuously distributed between the input and output ports of the current mirror and in which there is no obvious equivalent lumped two-transistor equivalent circuit. In contrast to

existing mirror circuits in which the matching-sensitive part of the circuit is comprised of two source-coupled transistors, the nonrectangular structures discussed in this dissertation are 4-terminal devices that can be viewed as dual-drain transistors. It will be shown that the proposed layout structures can be designed so that the mirror gain is less sensitive to linear parameter gradients than the widely used two-segment common centroid structures. The new structures are compared with conventional common centroid layouts for threshold voltage gradients at all angles across the active area of a mirror. Simulation results show significant improvements in matching characteristics of the proposed structures over what is achievable using existing layout techniques.

III. Dissertation Organization

The organization of this dissertation is based on a journal paper format. Chapter 1 contains a general introduction. Chapter 2 contains a summary of the existing approaches used to model matching performance. A new random parameter variation model will be proposed to resolve the inconsistency of the existing model. Chapter 2 will be submitted to IEEE Transactions on Circuits and Systems. Chapter 3 covers the design of a simulation tool called MOSGRAD. Measured results are presented to demonstrate the accuracy of the simulator. Chapter 3 will be also submitted to IEEE Transactions on Circuits and Systems. Chapter 4 introduces new layout techniques that exhibit reduced sensitivity to parameter gradients. Chapter 4 has been accepted as a paper by the Journal of Analog Integrated Circuits and Signal Processing. The final chapter contains general conclusion.

IV. References

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CHAPTER 2. IMPROVEMENT OF SIMULATION, PREDICTION AND REALIZATION OF PRECISION MATCHING-CRITICAL CIRCUITS

A paper to be submitted to the Journal of IEEE Transactions on Circuits and Systems

Mao-Feng Lan and Randall L. Geiger

Abstract

A new method for characterizing the effects of both the correlated and uncorrelated variations in semiconductor device properties on device matching is introduced. In contrast to existing approaches which focus on modeling the effects of process variations on either process or device parameters and then predicting matching performance from the ensuing device parameters, emphasis here is placed on directly modeling circuit-level matching characteristics in structures such as current mirrors or current source arrays. This approach circumvents the introduction of model errors inherent in existing approaches which are based upon the assumption that distributed parameter devices can be modeled with lumped parameter models. The lateral-dimensional effects of parameter variations throughout the channel region are shown to play an important role in matching characteristics in the presence of both parameter gradients and random parameter variations. Numerical results suggest a factor of 2 or more improvement in predicting matching performance in matching-critical applications over what is attainable with existing approaches is possible with the proposed method.

I. Introduction

Paralleling the increasing demand for high performance applications of image, voice and data transmission systems is the need for increased precision and performance in the underlying analog circuits embedded in these systems. Invariably these analog systems require close matching of current source arrays, precise control of current mirror gains or very low input referred offset voltages in differential amplifiers.

The issue of device matching has received considerable attention in the literature [1-9]. In several of these works, large amounts of experimental data was generated yet there were considerable discrepancies between predicted performance and actual measured performance. Although these discrepancies may not be of concern for low and medium resolution applications, they are of concern in systems where tight matching is required. These discrepancies are inherently attributable to limitations of the models used to predict the matching performance. This paper focuses on refining the models used to predicting matching performance and on using these refined models to more accurately predict the matching characteristics of key linear circuits. Specifically, we focus on characterizing the positional dependence of process and device parameters throughout the channel region of transistors, we discuss how this positional dependence affects the performance of matching-critical portions of linear circuits, we show that this positional dependence can be a significant factor affecting circuit performance, and we discuss strategies for minimizing the effects of this positional dependence on key linear building blocks.

II. Problem Formulation

Process parameters such as oxide thickness, doping profile, etc. are not constant either across a wafer or even across a die but rather vary with position on the die. For the purpose of characterizing the circuit level matching characteristics of linear blocks that are located in close proximity to each other on a die. these positionally dependent process parameters at a location (x,y) on the die can be viewed as random variables that can each be expressed functionally by the expression

$$P_i(x,y) = P_{iNOM} + P_{iPROC} + P_{iWAFER} + P_{iDIE}(x,y) + P_{iLOC}(x,y) + P_{iRAN}(x,y) \qquad (1)$$

where P_{iNOM} is the nominal value of the parameter P_i. The five remaining terms in (1) are themselves random variables that some authors choose to combine together into a single random variable. For notational convenience, the subscript "i" will be suppressed in the following discussions. The variable P_{PROC} characterizes the variation of the parameter P from one lot of wafers to another. The parameter P_{WAFER} characterizes the variation of P from one wafer to another wafer in a "lot" of wafers. The parameter P_{DIE} characterizes the variation of the parameter from one die location to another across a wafer and the parameter P_{LOC} characterizes the variation of the parameter in the neighborhood of the location where a matching-critical linear block (circuit) of interest lies. The variable P_{RAN} characterizes a random variation throughout the matching-critical linear block. The parameters P_{DIE}, P_{LOC} and P_{RAN} are position dependent. When modeled this way, the five random variables at the point (x,y) are nearly uncorrelated with each other. When considering devices in close proximity to each other on a die, the value of the random variables P_{PROC}, P_{WAFER} and P_{DIE} are nearly constant throughout the region and the random variable P_{LOC} can be modeled with

a parameter gradient (P_{GRAD}) at an angle θ_X by the expression

$$P_{LOC} = P_{GRAD}[(x-x_0)\cos\theta_x + (y-y_0)\sin\theta_x] \quad (2)$$

where P_{GRAD} and θ_x are random variables that are constant at the matching-critical circuit level but random at the die level. The parameter θ_x is relative to an arbitrary but fixed reference orientation on the die and (x_0,y_0) is an arbitrary but fixed reference point on the die. The position dependent random variables $P_{RAN}(x_1,y_1)$ and $P_{RAN}(x_2,y_2)$ are generally assumed uncorrelated for (x_1,y_1) and (x_2,y_2).

Device models are almost universally characterized by a set of model parameters. For a MOSFET, these model parameters include the threshold voltage (V_{T0}), the mobility (μ), the gate oxide capacitance density (Cox), etc. Some of these model parameters are determined from well-known relationships between the process parameters and others are more empirical in nature. Since the process parameters are position dependent, the model parameters are position dependent as well and thus since the underlying process parameters are stochastic, the model parameters are stochastic. Although many of the process parameters are uncorrelated or weakly correlated, a single process parameter often affects more than one model parameter causing correlation between the model parameters. This correlation is often neglected when characterizing the matching characteristics of matching-critical linear circuits and will be neglected in this work as well. Following this standard approach for characterizing the process parameters, the device model parameters can be expressed in the form

$$\gamma(x,y) = \gamma_{NOM} + \gamma_{PROC} + \gamma_{WAFER} + \gamma_{DIE}(x,y) + \gamma_{LOC}(x,y) + \gamma_{RAN}(x,y) \quad (3)$$

When considering devices in close proximity to each other on a die, the value of the random

model variables γ_{PROC}, γ_{WAFER} and γ_{DIE} are nearly constant throughout the region and the random variable γ_{LOC} can be modeled as a parameter gradient (γ_{GRAD}) at an angle θ by the expression

$$\gamma_{LOC}(x,y) = \gamma_{GRAD}(x_0,y_0)\cdot[(x-x_0)\cos\theta(x_0,y_0) + (y-y_0)\sin\theta(x_0,y_0)] \quad (4)$$

where $\gamma_{GRAD}(x_0,y_0)$ and $\theta(x_0,y_0)$ are random variables that are constant at the matching-critical circuit level but random at the die level. As with the process variables, the positionally dependent random variables $\gamma_{RAN}(x_1,y_1)$ and $\gamma_{RAN}(x_2,y_2)$ are uncorrelated for (x_1,y_1) and (x_2,y_2).

The introduction of position-dependent model parameters for the purpose of ultimately modeling the statistical characteristics of the MOS transistor is widely used [1-9]. In these works, it is assumed that the actual value (sometimes termed the nominal value) of the lumped model parameters for a device located in close proximity to the location (x_A, y_A) can be obtained by integrating the position-dependent model parameters over the two-dimensional area of the channel

$$\gamma(x_A,y_A) = \frac{1}{Area}\iint_{Area}\gamma(x,y)dxdy \quad (5)$$

We will refer to this as the lumped parameter derivation from a distributed parameter domain as the parameter averaging approach to modeling or equivalently as the integral model throughout this paper. The parameter averaging mapping of (5) from a distributed stochastic parameter domain to a single lumped parameter $\gamma(x_A,y_A)$ has been used for so long that the issue of the validity of this mapping is generally not questioned. Correspondingly, a mapping from the distributed parameter domain $\gamma(x,y)$ to a single lumped parameter is

needed if existing lumped device models, such as those used in the popular SPICE-type simulators, are to be utilized.

In matching-critical circuits such as current mirrors or differential amplifiers, the parameters γ_{PROC} and γ_{WAFER} are constant at the die level and do not substantially contribute to mismatch. The standard approach for managing/minimizing the effects of γ_{DIE} is to place matching sensitive components in close proximity on the die. The standard approach for managing/minimizing the effects of γ_{LOC} is to use layout strategies such as interdigitzation or common centroiding to cancel these effects. Finally, the standard approach for managing/minimizing the effects of the random variables γ_{RAN} is to allocate sufficient area to the critical devices to take advantage of the fact that they are positonally uncorrelated. Using the integral model of (5), it can be shown that the standard deviation of $\gamma_{RAN}(x_A,y_A)$ decreases with the square root of the active area. Thus, with matching-critical components in close proximity on a die, the variables γ_{PROC}, γ_{WAFER} and γ_{DIE} have negligible effects on matching. The matching performance is strongly dependent upon how γ_{LOC} and γ_{RAN} manifest themselves at the circuit level in matching-critical circuits. The balance of this paper focuses on the effects of γ_{LOC} and γ_{RAN} on matching performance in the specific case where the parameter γ is the threshold voltage. The issues surrounding the mapping of the threshold voltage from a distributed parameter domain to a lumped parameter apply directly to other distributed model parameters as well.

III. Modeling Gradient and Random Effects in Matching-Critical Circuits

A good model for the active devices is essential for accurately predicting matching characteristics of matching-critical circuits. Since both gradient effects and random fluctuations in device parameters are known to play key roles in matching performance, it is particularly important that the device models effectively incorporate these fluctuations. Essentially all works on device matching appearing in the literature follow the approach of using the integral model of (5) to map a distributed parameter space to a lumped parameter set. These lumped parameters are then used in the existing device models. The approach is used for characterizing the effects of both systematic fluctuations and random variations. Unfortunately, none of these works prove that mapping is valid or even question the validity of the mapping.

We will now show that the lumped parameter mapping of (5) can result in substantial modeling errors which, in turn, can introduce substantial errors in simulations of matching-critical circuits that use these models. The invalidity of this mapping and correspondingly the potential magnitude of the modeling errors associated with this mapping can be demonstrated by considering the non-conventional transistor depicted in Fig. 1a by looking at the affects of a single positionally dependent model parameter, the threshold voltage. In this figure, it will be assumed that d is very small compared to L so that the channel region is decomposed into two parts, the left part of area A_1 and termed the A_1 region and the right part of area A_2 and termed the A_2 region. If it is assumed that the threshold voltage in the A_2 region is V_{T2} and in the A_1 region it is V_{T1}, it follows from the integral model (5) that the equivalent threshold voltage of the device is

$$V_{TEQ} = \frac{A_1 V_{T1} + A_2 V_{T2}}{A_1 + A_2} \qquad (6)$$

If $A_2 >> A_1$ it follows from (6) that the threshold voltage can be expressed as $V_{TEQ} \approx V_{T2}$. However, when the distance d is small compared to the length L, almost no current flows in the A2 region and thus the actual device will have a threshold voltage of $V_{TEQ} \approx V_{T1}$. It is apparent from this example that the parameter averaging mapping of (5) can result in large model errors. The structure of Fig. 1a is admittedly an impractical transistor layout but does demonstrate that the parameter averaging mapping can lead to substantially erroneous results. This example does, however, raise the question about whether the integral model of (5) is adequate for predicting matching performance in the presence of parameter gradients in more practical structures where precision is required and it suggests that a re-examination of results obtained using the integral model to predict matching performance is needed.

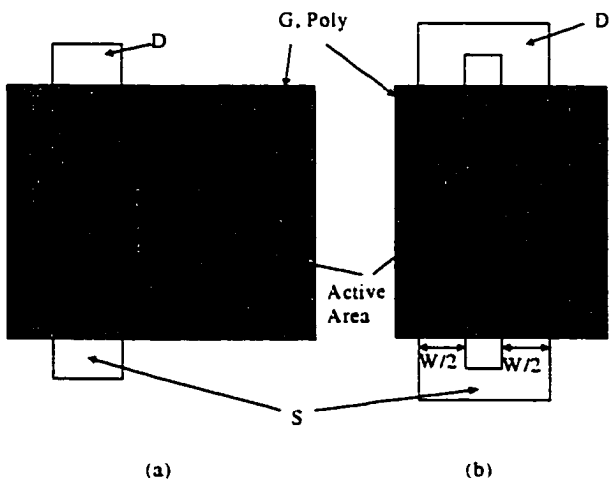

Fig 1. Non-conventional transistor

The issue of model consistency is also of concern. *We define a device model to be consistent if alternative but equivalent representations of a device by the model result in equivalent device performance. If equivalent representations of a device by a model predict different performance, we say the model is inconsistent.*

We will now show that the integral model of (5) is inconsistent as well. To see this, consider the parallel connection of two MOS transistors as depicted in Fig. 1b where the transistor on the left is assumed to have threshold voltage V_{T1} and the transistor on the right is assumed to have threshold voltage V_{T2}. If we treat the device as a single transistor operating in the saturation region and apply the integral model of (5), it follows that the equivalent threshold voltage is

$$V_{TEQ} = \frac{V_{T1} + V_{T2}}{2} \tag{7}$$

To separate the effects of errors introduced by the parameter averaging of (5) from model errors and to keep model complexity from obscuring the effects of parameter averaging, a simple and consistent model will be used. If bulk effects on the threshold voltage are neglected, it can be shown that the transistor model as characterized in the saturation region and the triode regions respectively by the following expressions is consistent.

$$I_D = \frac{\mu C_{OX} W}{2L}(V_{GS} - V_T)^2 \tag{8a}$$

$$I_D = \frac{\mu C_{OX} W}{L}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS} \tag{8b}$$

With the integral model of (5), it follows from (7) and (8a) that the saturation region current of the parallel connection of Fig. 1b is given by

$$I_{D-Integral\ Model} = \frac{\mu C_{OX} W}{2L}(V_{GS} - (\frac{V_{T1} + V_{T2}}{2}))^2 \quad (9)$$

If, however, an alternate representation is considered in which we treat the parallel connection as two separate devices and use the integral model of (5) to obtain the equivalent threshold voltage of each of the devices, it follows trivially that $V_{T1EQ}=V_{T1}$ and $V_{T2EQ}=V_{T2}$. Thus, using the same square law model we obtain the three equations

$$I_{D1} = \frac{\mu C_{OX} W}{2L}(V_{GS} - V_{T1})^2 \quad (10)$$

$$I_{D2} = \frac{\mu C_{OX} W}{2L}(V_{GS} - V_{T2})^2 \quad (11)$$

$$I_D = I_{D1} + I_{D2} \quad (12)$$

These equations can be solved to obtain

$$I_D = \frac{C_{OX} W}{2L}((V_{GS} - \frac{V_{T1} + V_{T2}}{2})^2 + (\frac{V_{T1} - V_{T2}}{2})^2) \quad (13)$$

Since I_D as modeled by (9) differs from I_D as modeled by (13) if $V_{T1} \neq V_{T2}$, it follows that the integral model of (5) is inconsistent. Although the examples discussed here have focused on deterministic variations in the threshold voltage, it will be shown later that the integral model introduces errors in predicting the affects of random variations in parameters as well.

The source of errors in using the integral model should be apparent from the preceding examples. Central to the use of the integral model for mapping a distributed parameter domain to a lumped parameter is the explicit assumption that the functional form of the device models remains fixed in the presence of parameter variations. It can be seen from the preceding example that the functional form of the device characteristics depends upon how the device is represented with different representations having different functional

relationships between the port variables. As a consequence, there does not exist a consistent finite-dimensional lumped parameter model for a MOS transistor that is applicable for arbitrary parameter distributions in the channel region.

We will also show that the integral model is not consistent with experimental results. From the integral model. it is apparent that the effects of random parameter variation on parameter extraction are independent of the current or device orientation. Experimental data relating to device orientation and matching was presented in [3]. Although these results show no significant shift in the averages of the current factor, $\beta=(\mu C_{OX}W/L)$, between parallel and 90° rotated transistors, the standard deviation of β is significantly affected by the orientation as shown in the experimental data which is repeated here in Fig. 2. This data indicates the mismatch in β is affected by device orientation in contrast to the independence predicted by the integral model. The authors of [3] suggested that the effect observed in Fig. 2 was due to local mobility variations presumably the $\gamma_{LOC}(x,y)$ dependence of (2). One can argue that the local variation noted in [3] is typical of the variation of other parameters across the active region of a distributed device. By using the integral model in extracting lumped model parameters, the information about the local variations will be suppressed or skewed.

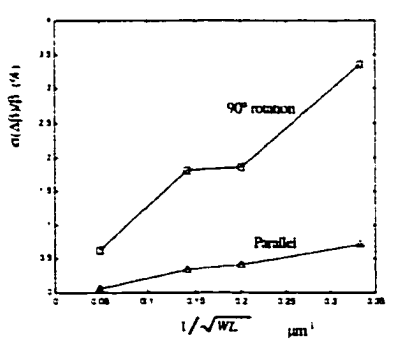

Fig. 2 Standard deviation of β with parallel and rotated placement (from Fig. 4b of [3])

Even though the integral model of (5) results in model errors and is inconsistent, the model is still useful for predicting the effects of parameter variations in many applications. In what follows we will attempt to quantify more practically the magnitude of the errors expected when using the integral model and then discuss layout strategies for enhancing matching performance that are obscured by the integral model.

We will consider separately the modeling of the effects of γ_{LOC} and γ_{RAN} on the performance of matching-critical circuits. When considering the effects of γ_{LOC}, we will assume that the matching critical area is sufficiently small that the linear gradient model of (4) can be used to model γ_{LOC}. In an attempt to keep the length of this discussion manageable, we will focus exclusively on the effects of a spatially distributed threshold voltage. In many matching-critical circuits this plays the dominant role in limiting matching performance.

IV. Gradient Effects on Matching

Fig. 3 shows four representations of the commonly used rectangular layout of a single MOS transistor. For discussion purposes, it will be assumed that there is a linear gradient in the threshold voltage from source to drain (i.e. $\theta = 90°$ relative to the gradient reference, O, in Fig 3). The standard representation is shown in Fig. 3a. Alternate representations of two devices in parallel each of width W/2 and length L, of two devices in series each of width W and length L/2, and of 10 devices in series each of width W and length L/10 are also shown. We will now consider the limitations of the integral model on the rectangular transistor in the presence of a vertical gradient. The drain currents in the four representations of the device are designated as I_{D1}, I_{D2}, I_{D3} and I_{D4} respectively and all four representations are assumed to

have identical gradient effects and an identical reference point. As a special case of (4) with $\theta = 90°$, the linear gradient in the threshold voltage is modeled as

$$V_T(x,y) = V_{T0} + yV_{TGRAD} \tag{14}$$

where the coefficient V_{TGRAD} is the magnitude of the gradient and V_{TO} is the threshold voltage at the point O in Fig. 3. As expected, if $V_{TGRAD} = 0$, and the device is assumed to be operating in the saturation region, all four currents are equal and given by

$$I_D = \frac{\mu C_{OX} W}{2L}(V_{GS} - V_{T0})^2 \tag{15}$$

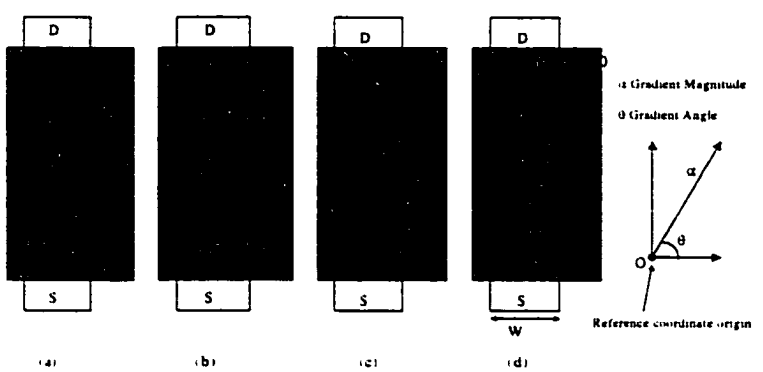

Fig 3. Rectangular MOS transistor a) Single channel b) Two parallel devices c) Two series devices d) 10 Series devices

If $V_{TGRAD}=0$, and the parameter averaging model of (5) is used to obtain V_T for the four representations, it follows from (5) and (14) that $V_T = V_{TO}$ for the representation of Fig. 3a. Thus the drain current I_{DI} is still given by (15). An analysis of the remaining structures is more tedious. A simple well-known theorem does, however, help in the evaluation of the integral of (5) when the gradient is linear. In the context of the parameter γ for a device in the vicinity of the point (x_A,y_A) in the integral model this theorem is:

Theorem 1 If $\gamma(x,y)$ is linearly dependent upon the variables x and y, then $\gamma(x_A,y_A)=\gamma(x_{A0},y_{A0})$ where (x_{A0},y_{A0}) is the geometric centroid of the channel region and $\gamma(x_A,y_A)$is the lumped value of the parameter as defined by the integral model of (5).

It follows from this theorem that for the representation of Fig. 3b, the left and right transistors both have threshold voltages of V_{T0} and thus he left and right transistors both have drain currents given by

$$I_{Dk}=\frac{\mu C_{OX}(\frac{W}{2})}{2L}(V_{GS}-V_{T0})^2 \qquad k\in\{-1,1\} \tag{16}$$

Adding the two drain currents, we obtain the drain current given by (15).

In the representation of Fig. 3c, it follows from Theorem 1 and (5) that the lower and upper transistors have threshold voltages of

$$V_{Tk}=V_{T0}+(2k\text{-}3)V_{TGRAD}\frac{L}{4} \qquad k\in\{1,2\} \tag{17}$$

Although the overall device is in the saturation region, the lower transistor in the series connection is operating in the triode region and its current is given by the expression (8b). Substituting the expressions for V_T from (17) into (8a) and (8b), we obtain the expressions

$$I_D=\frac{\mu C_{OX}W}{L}(V_{GS2}-V_{T2})^2 \tag{18}$$

$$I_D=\frac{\mu C_{OX}2W}{L}(V_{GS}-V_{T1}-\frac{V_{DS1}}{2})V_{DS1} \tag{19}$$

$$V_{GS}=V_{DS1}+V_{GS2} \tag{20}$$

A straightforward manipulation of the expressions of (18)-(20) to eliminate V_{DS1} and V_{GS2} yields the expression

$$I_{D3}=\frac{\mu C_{OX}W}{2L}\left(\frac{(V_{T1}-V_{T2})}{\sqrt{2}}+\sqrt{(V_{GS}-(\frac{V_{T1}+V_{T2}}{2}))^2+(V_{T1}-V_{T2})(V_{GS}-(\frac{V_{T1}+V_{T2}}{2}))+(\frac{V_{T1}-V_{T2}}{2})^2}\right)^2 \quad (21)$$

Substituting from (17) into (21), we obtain

$$I_{D3}=\frac{\mu C_{OX}W}{2L}\left(-\frac{LV_{TGRAD}}{2\sqrt{2}}+\sqrt{(V_{GS}-V_{T0})^2-(\frac{LV_{TGRAD}}{2})(V_{GS}-V_{T0})+(\frac{LV_{TGRAD}}{4})^2}\right)^2 \quad (22)$$

In the fourth representation depicted in Fig. 3d, the transistors from bottom to top have threshold voltages of

$$V_{Tk}=V_{T0}+(2k\text{-}11)V_{TGRAD}\frac{L}{20} \quad k\in\{1,2,3,4,5,6,7,8,9,10\} \quad (23)$$

In this case, M1-M9 are operating in the triode region and characterized by equation (8b) and M10 is operating in the saturation region characterized by equation (8a). The relationship between the drain-source voltage and gate-source voltage for the kth transistor is given by

$$V_{GSk}=V_{GS}-\sum_{i=1}^{9}V_{DSi} \quad (24)$$

This results in a set of 11 equations which can be solved simultaneously to find the drain current for the fourth representation in Fig. 3d, I_{D4}. An expression for the drain current in this case is unwieldy with a functional dependence upon V_{GS} that differs considerably from that of (8b).

With the vertical gradient angle (θ=90° in Fig 3), the functional dependence upon the port voltages for I_{D3} and I_{D4} differ considerably from that from I_{D1}. At other gradient angles, the equal potential surfaces in the channel are not horizontal lines making it difficult to

precisely analyze the segmented structures. If, however, the gradient magnitude is reasonably small, the segmented models give very good approximations and it follows from the integral model of (5) and Theorem 1 that the threshold voltages for the segmentations of Fig. 3b, Fig. 3c and Fig. 3d are given respectively by the expressions

$$V_{Tk} = V_{T0} + V_{TGRAD}((2k-1)\frac{W}{4}\cos\theta) \quad k \in \{1,2\} \tag{25}$$

$$V_{Tk} = V_{T0} + V_{TGRAD}(\frac{L}{4}(2k-1)\sin\theta) \quad k \in \{1,2\} \tag{26}$$

$$V_{Tk} = V_{T0} + V_{TGRAD}(\frac{L}{20}(2k-11)\sin\theta) \quad k \in \{1,2,3,4,5,6,7,8,9,10\} \tag{27}$$

Thus, for arbitrary gradient angles, there is also considerable difference in the functional form for I_{D1}, I_{D2}, I_{D3} and I_{D4} if the integral model of (5) is used.

To obtain an appreciation for the magnitude of the error introduced by the parameter averaging assumption of (5) define the model discrepancy by the expression

$$H_k = \frac{I_{Dk} - I_{D1}}{I_{D1}} 100\% \tag{28}$$

Fig. 4 shows a plot of H_k as a function of V_{TGRAD} with a vertical gradient (θ=90°) for V_{DS}=5V, V_{GS}=2.5V, V_{TO}=0.8V, W=40μm, and L=40μm for the segmentations of Fig. 3c and Fig. 3d. For with a gradient of V_{TGRAD} = 0.5mV/μm, the discrepancy for the 2-element vertical segmentation is about 0.25% and for the 10-element segmentation it is about 0.38%. These discrepancies introduced by the parameter averaging assumption are causing modeling errors in current levels that are over 1 LSB at the 8-bit level.

The discrepancy as defined by (28) compares the current in a vertically segmented transistor to that in an unsegmented transistor. The fact that there is a difference between the

predicted current for a single transistor representation and for the segmented transistor representations of the same device is apparent and the difference becomes significant at even relatively low bit levels. The question naturally arises about whether the single transistor model or the multiply segmented transistor model will more accurately predict actual current levels in the presence of parameter gradients or even whether either model is sufficiently accurate to predict matching performance of matching-sensitive circuits. More importantly, however, is the issue of whether the discrepancies in current inherent in the parameter averaging model will adversely affect predictions of matching performance in matching-critical circuits such as current mirrors, differential amplifiers, etc.

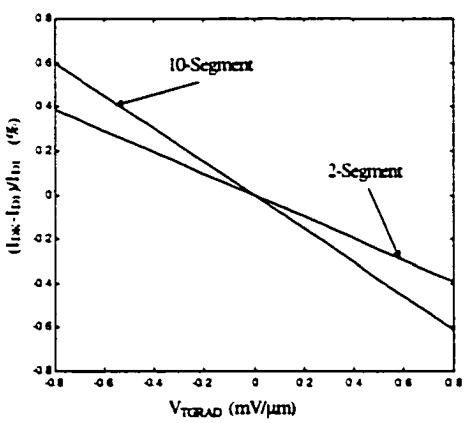

Fig. 4 Model discrepancy introduced from (5)

To address the latter issue, we will consider the two layouts of a matching-critical circuit, specifically of the current mirror of Fig. 5 shown in Fig. 6. A simple layout is shown in Fig. 6a and a two-segment common centroid layout is shown in Fig. 6b. A two-dimensional simulator MOSGRAD that incorporates arbitrary parameter gradients throughout the channel region [10] was used to compare the performance of the matching-

critical circuits. The model error is defined by error equation

$$E = \frac{M_{INTEGRAL} - M_{ACTUAL}}{M_{ACTUAL}} 100\% \tag{29}$$

where M_{ACTUAL} is the actual mirror gain and $M_{INTEGRAL}$ is the mirror gain predicted by the integral model.

For notational convenience, the reference point will be established at the geometric centroid of the channel regions. To concentrate specifically on the model errors, it is assumed that the spacing D_H and D_S in these layouts are minimum not against the design law as 4μm and 6μm respectively. With this notation, it follows from the integral model for the simple layout that,

$$V_{T1} = V_{T0} - V_{TGRAD}\left(\frac{W}{2} + \frac{D_H}{2}\right)\cos\theta \tag{30}$$

$$V_{T2} = V_{T0} + V_{TGRAD}\left(\frac{W}{2} + \frac{D_H}{2}\right)\cos\theta \tag{31}$$

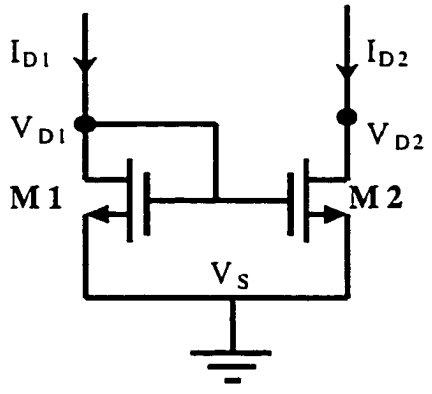

Fig. 5 Basic current mirror circuit

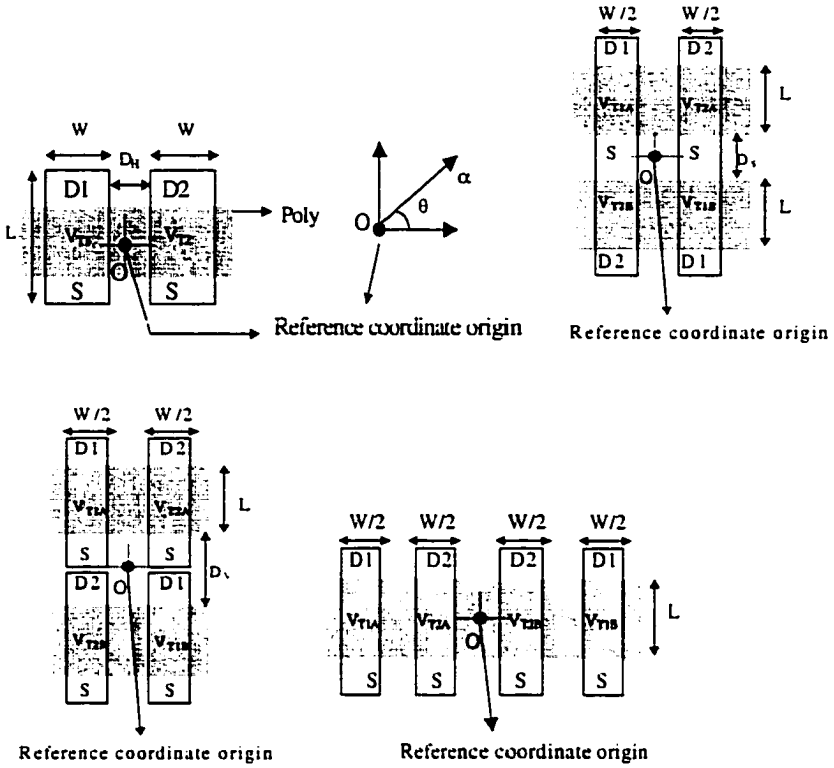

Fig. 6 Current mirror circuit layouts a) Simple b) 2-Segment common centroid with common source c) 2-Segment common centroid with common orientation d) Interdigitized

For the common centroid layout, if M_1 and M_2 are treated as single devices, it follows that

$$V_{T1} = V_{T2} = V_{T0} \tag{32}$$

If M_1 and M_2 are treated as devices with two segments, it follows that

$$V_{T1A} = V_{T0} - V_{TGRAD}\left(\frac{W}{4} + \frac{D_H}{2}\right)\cos\theta + V_{TGRAD}\left(\frac{D_S}{2} + \frac{L}{2}\right)\sin\theta \tag{33}$$

$$V_{T1B} = V_{T0} + V_{TGRAD}\left(\frac{W}{4} + \frac{D_H}{2}\right)\cos\theta - V_{TGRAD}\left(\frac{D_S}{2} + \frac{L}{2}\right)\sin\theta \tag{34}$$

$$V_{T2A} = V_{T0} + V_{TGRAD}(\frac{W}{4} + \frac{D_H}{2})\cos\theta + V_{TGRAD}(\frac{D_S}{2} + \frac{L}{2})\sin\theta \quad (35)$$

$$V_{T2B} = V_{T0} - V_{TGRAD}(\frac{W}{4} + \frac{D_H}{2})\cos\theta - V_{TGRAD}(\frac{D_S}{2} + \frac{L}{2})\sin\theta \quad (36)$$

The issue of the magnitude of the gradients that will be experienced in a typical process is difficult to address since good gradient data is not widely available. Some works suggest an average gradient in the range of 10μV/μm is typical whereas others show gradients are highly dependent on the position on a die [9] and are in the 1mV/μm range or larger. It can be argued that if worst case gradients were consistently in the 10μV/μm range, the need for using common centroid layout techniques would be essentially nonexistent in almost all practical applications since the random variations would completely dominate gradient effects. It can also be argued that if a respectable yield is to be achieved, matching-critical circuits must perform acceptably even when they are physically positioned on portions of the die that have large gradients. In what follows we will assume a gradient of 0.5mV/μm in the threshold voltage. This is well above the average value reported but well below what was present at many locations throughout the test devices studied [9]. The results that follow will be even more dramatic if larger gradients are present.

Table 1 shows quantitatively the effects of model errors in the current mirrors of Fig. 6a and Fig. 6b for a gradient of magnitude 0.5mV/μm at an angle of θ=45°, a threshold voltage of 0.8V, V_G=V_{D1}=2.5V and V_{D2}=2.5 to eliminate output impedance effects. The devices are all of length 40μm. The width of the devices was assumed to be 40 μm for the simple layout and each was of width 20 μm for the common centroid layout. The table shows two different simulated mirror gains for the common centroid layout. The first is based upon

the assumption that the integral equation of (5) can be applied directly to M1 and M2 and the second based upon the assumption that M1 and M2 each have the two segments. The data in Table 1 shows the errors associated with the integral model for the 45°gradient with a fixed device size and a fixed gradient magnitude. From the data presented, it appears the integral model of (5) is useful for predicting the effects of parameter gradients when low to medium matching performance is required but in high performance applications, the integral model is not effective at predicting performance.

Table 1 Model errors in mirror gain for linear gradients

	$M_{Integral}$	M_{Actual}	Error (%)
Simple	0.9819	0.9826	-0.07124
Common Centroid			
Single Segment	1	1.00005169	-0.005169
Two Segment	1.00004567	1.00005169	-6.02e-4

The angle of the gradient is a random variable and, as such, the matching performance as a function of the angle of the gradient is of concern. For high yield, it is necessary to keep the errors in the most unfavorable angle below an acceptable threshold. Correspondingly, measurement results on small sample sizes can be unrealistically optimistic if a favorable gradient direction occurs. For these reasons, an understanding of the mismatch effects as a function of gradient angle for different layout structures is of interest. Two additional popular layouts of a current mirror are added to Fig. 6 and shown in Fig. 6c and Fig. 6d. Thus the four

layouts in Fig. 6 include a simple layout and three two-segment common-centroid layouts. The second structure, Fig. 6b, is a diagonally symmetric structure with a common source region and the third, Fig. 6c, is a diagonally symmetric structure with common device orientation. The last common-centroid layout, Fig. 6d, is often termed an interdigitized layout. For comparative purposed. all are assumed to have the same effective W and L and the same gate area. Simulation results for the accuracy of the current mirror gain of the four structures based upon the MOSGRAD simulator as a function of the angle of the gradient are shown in Fig. 7 and the simulation results for common centroid layouts are expanded into Fig. 8 where mismatch is defined as $100\%(I_{D2}-I_{D1})/I_{D1}$ when $V_{D1}=V_{D2}$. In these simulations, it was assumed that the threshold voltage at the geometric centroid of all structures was 800mV, the threshold gradient magnitude was 0.5mV/μm, L=20μm, W=10μm, D_H=4μm, D_S=6μm and D_V=12μm.

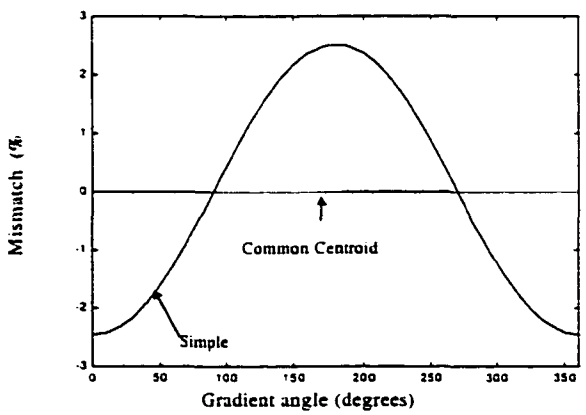

Fig. 7. Comparison of systematic mismatch for simple and common centroid layouts

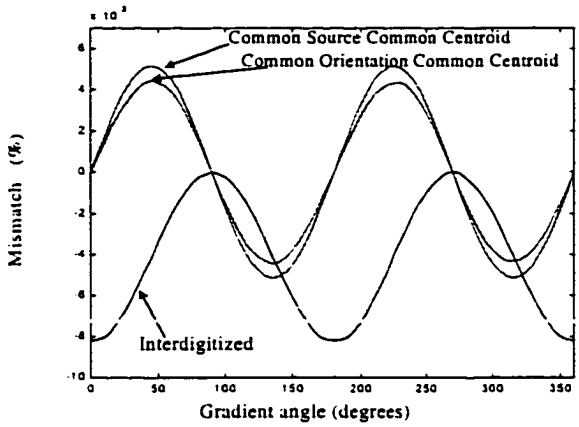

Fig. 8. Comparison of interdigitized and common centroid layouts in closer detail

V. Inconsistency with Existing Random Variation Model

The effects of random parameter variations of channel-dependent process parameters on matching of current mirrors and offset voltage of operational amplifiers, specifically the standard deviation of the corresponding matching parameter, has been modeled for many years by a reciprocal of the square root of the area relationship referred as the law of area. If it is assumed that equivalent model parameters can be obtained with the integral equation of (5), it is easy to show that the standard deviation of the parameter variations for a given process can be expressed in terms of process-related area proportionality constants [3] that are commonly referred to as A_{VTO}, A_{μ}, and A_{COX}, etc.. The major contributor to random variations in current mirror gains and random variations in input-referred offset voltage for most practical layouts in current MOS processes is the random threshold voltage variations. For this reason, we will limit the discussion in this section to the effects of random variations in the threshold voltage on circuit performance. The widely accepted reciprocal area relationship for the variance of V_T of a rectangular device of length L and width W is given

by the equation

$$\sigma^2(V_T) = \frac{A_{VT}^2}{WL} \tag{37}$$

We have intentionally used the parameter A_{VT} instead of the more widely used parameter A_{VTO} to avoid possible confusion since some authors have used the parameter A_{VTO} to characterize the variance of the threshold voltage of a single rectangular device whereas others have used the same parameter to characterize the variance of the difference in threshold voltages of two devices that are nominally matched. We use the parameter $A_{\Delta VT}$ to characterize the variance of the difference in the threshold voltage of two devices each of area W·L. It follows that the relationship between A_{VT} and $A_{\Delta VT}$ can be expressed as

$$A_{\Delta VT} = \sqrt{2} A_{VT} \tag{38}$$

If the standard Schickman-Hodges model of (8) is used to model the MOS transistor and if the integral model of (5) is used to obtain the lumped value for the threshold voltage, it can be shown that the relative standard deviation of drain current of a single transistor, $\sigma(I_D)/I_D$ is given by the well known expressions

$$\frac{\sigma^2(I_D)}{I_D^2} = \frac{\sigma^2(V_T)}{(V_{GS} - V_{TN} - \frac{1}{2}V_{DS})^2} \qquad \text{for } V_{DS} < V_{GS}\text{-}V_{TN} \tag{39}$$

$$\frac{\sigma^2(I_D)}{I_D^2} = \frac{4\sigma^2(V_T)}{(V_{GS} - V_{TN})^2} \qquad \text{for } V_{DS} \geq V_{GS}\text{-}V_{TN} \tag{40}$$

A single transistor of length L and width W is shown in Fig. 9a and an alternative and equivalent representation is shown in Fig. 9b. In the equivalent representation, the transistor is decomposed into a series connection of N transistors each of length L/N. Based upon the integral model, the threshold voltage variance of each of the N transistors can be obtained

directly from (37) which, in this case, becomes

$$\sigma^2(V_{Ti}) = \frac{A_{VT}^2}{W(L/N)} \qquad i=\{0,1,2,\ldots,N-1\} \tag{41}$$

If the model for $\sigma^2(V_T)$ given by (37) is valid, then the equivalent N-segment representations modeled by (41) should predict the same statistical circuit performance for any circuit using the MOSFET for any N. A circuit comprised of a single MOS transistor biased with voltage sources between gate and source and between drain and source was constructed. The output variable was defined to be the drain current I_D. Monte Carlo simulations of the relative standard deviation of the drain current, $\sigma(I_D)/I_D$, due to random threshold variations for a device with W=100μm, L=100μm, and A_{VT}=10mV·μm were run for different values of N with the square-law device model of (8) in both Matlab and Hspice. The results of the simulations were essentially the same and are shown in Fig. 10. In these simulations, it was assumed that V_{GS}=2.5V, V_{DS}=1.7V, and V_{TN}=0.8V. The results of Fig. 10 show that the relative standard deviation of the drain current is dependent upon N, in contradiction to what happens in a real device and in contradiction to the independence on N that must be exhibited if the model of (37) is valid. The value of $\sigma(I_D)/I_D$ predicted by (40) agrees with the simulation results for N=1 but for even small values of N, considerable discrepancies exist. Not only is $\sigma(I_D)/I_D$ dependent upon N, but it diverges to infinity as N becomes large. These results show use of the integral model to predict the effects of random parameter variations is both invalid and inconsistent. Although the inconsistencies in the integral model have not been reported in the literature, experimental results that have been presented do suggest problems with the integral model as well. These are evidenced, in part, by poor fits of a line

through reported $\sigma(V_T)$ vs $1/\sqrt{WL}$ plots, by fits that do not pass through the origin of the $\sigma(V_T)$ vs $1/\sqrt{WL}$ plane [3], and more recently [11] by extracted values for A_{VT} that differ considerably between rectangular and hexagonal transistors.

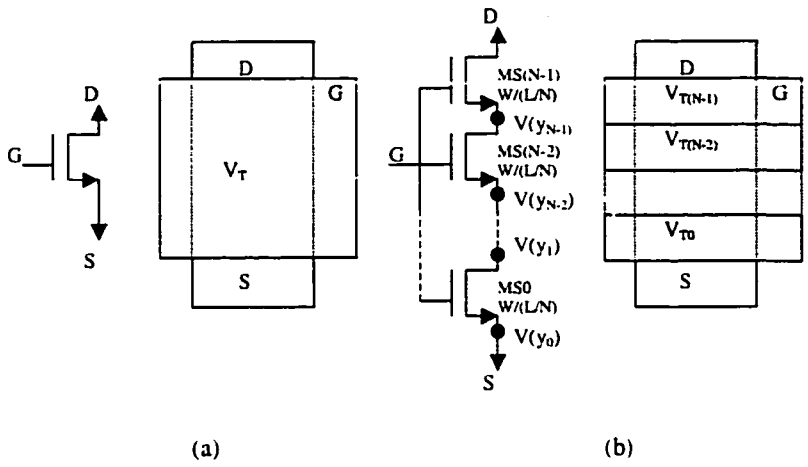

Fig 9. Two equivalent representations of a transistor
a) Single segment, b) N-Segment

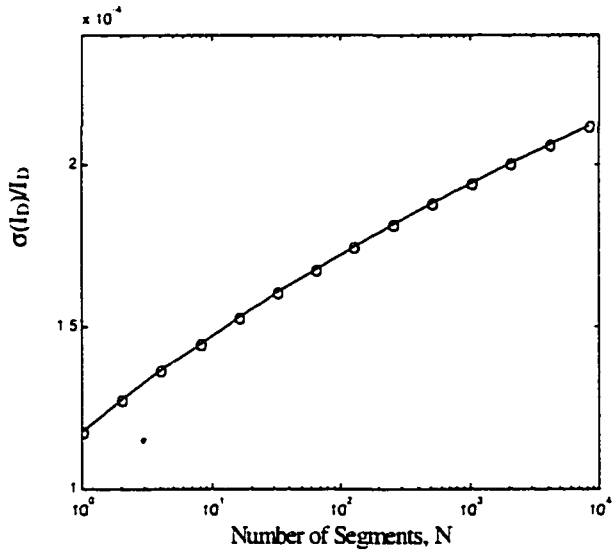

Fig 10. $\sigma(I_D)/I_D$ using the model (41)

VI. Consistent Model for Random Parameter Variations

In the traditional approach, the random model parameters are extracted directly from I/V device measurements based upon the lumped model of (39) and (40). With the assumption that the integral model characterizes the equivalent model parameters, a model for the random parameter variance that is characterized by a single model parameter, such as A_{VT}, and depends only upon the reciprocal of the channel area was derived. This model was fit to the measured data to obtain the model parameter A_{VT}. This approach which showed a reciprocal area dependence of the variance of the threshold voltage was reassuring since the randomness in processing such as the randomness in the position of ions implanted in a channel region or the randomness of impurities during crystal growth also show a reciprocal area dependence on the variance. Unfortunately, this approach resulted in an inconsistent model which diverged when the model was applied to a segmented transistor.

In an attempt to obtain a more accurate model of the effects of random variations in the threshold voltage on circuit performance, we will retain the assumption that the variance of the threshold voltage exhibits a reciprocal area dependence but revisit how this process parameter affects the device performance by returning to the gradual channel approximation which was used to obtain the I-V characteristics of the device. For convenience, the device is assumed to be rectangular. A cross section of a device operating in saturation is shown in Fig. 11a. For notational convenience, it will be assured that the reference node is the source and thus $V_{GS}=V_G$ and $V(ys)=V(y)$.

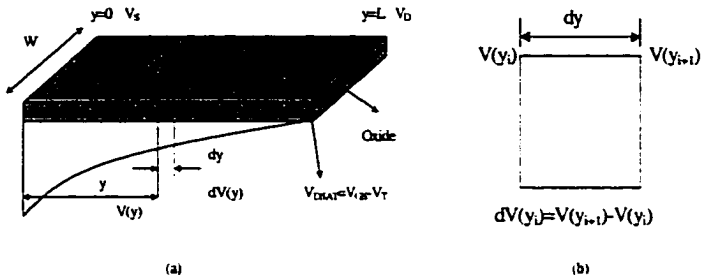

Fig. 11 Cross section of a device

In the gradual channel approximation, the differential channel voltage relates to the differential channel conductance by the relationship

$$dV(ys) = \frac{I_D}{dC(y)} \tag{42}$$

where V(ys)=V(y)-V_S=V(y) and dC(y) is the differential channel conductance. The differential channel conductance relates to the channel density in the channel by the relationship

$$dC(y) = \frac{\mu W Q(y)}{dy} \tag{43}$$

where Q(y) is the channel charge density and μ is the carrier mobility. The relationship between drain current and channel charge density is readily obtained from (42) and (43) as

$$I_D dy = \mu W Q(y) dV(y) \tag{44}$$

and the channel charge density relates to the gate oxide capacitance density, C_{OX}, for a n-channel device by the relationship

$$Q(y) = C_{ox}(V_{GS} - V_T - V(y)) \tag{45}$$

Equations (42)-(45) can be combined into the single differential equation

$$I_D dy = \mu C_{ox} W(V_{GS} - V_T - V(y))dV(y) \tag{46}$$

This equation can be readily solved by integration from 0 to y to obtain the standard expression for I_D in both the saturation and triode regions.

$$I_D = \frac{W\mu C_{ox}}{y}((V_{GS} - V_T)V(y) - \frac{V(y)^2}{2}) \qquad 0<y<L \tag{47}$$

Since (47) is valid for all $0 \leq y \leq L$ in both the triode and saturation regions, it follows that the triode region model for the device is

$$I_D = \frac{W\mu C_{ox}}{L}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS} \tag{48}$$

If the device is operating in the saturation region, it follows from (47) with $V(ys)=V_{DSAT}=V_{GS}-V_T$ that

$$I_D = \frac{W\mu C_{ox}}{2L}(V_{GS} - V_T)^2 \tag{49}$$

By solving (47) and (49), the channel voltage at position y in the channel when operating in saturation, V(y), can be expressed as

$$V(y) = (V_{GS} - V_T)(1 - \sqrt{1 - \frac{y}{L}}) \tag{50}$$

The effects of random variations in V_T on the drain current will now be investigated. If the threshold voltage is non-stochastic, the process parameter V_T is also a model parameter. If the process threshold voltage becomes stochastic, the effects of V_T on the model also become stochastic. If the same variable is used for both the process threshold voltage and the model threshold voltage, the variables are inherently assumed to be identical and thus have identical probability density functions. If this assumption is made and if it is assumed that the variance of V_T has a reciprocal area dependence, it was shown that the resultant device model

was inconsistent. Thus, the question naturally arises – Is the process threshold voltage identical to the model threshold voltage? To address this question, in this section the variable V_T will refer to the process threshold voltage and V_{TM} will refer to the model threshold voltage. The process threshold voltage for a n-channel transistor will be defined by the relationship

$$Q_A = C_{ox}(V_{GC} - V_T)A \tag{51}$$

where Q_A is the channel charge in a channel region of area A and V_{GC} is the gate-channel voltage which is assured constant throughout the channel region. It will be assured that the random variable V_T has a mean V_{TN} and a variance given by

$$\sigma_{VT}^2 = \frac{\tilde{A}_{VT}^2}{A} \tag{52}$$

where $\tilde{A}_{VT}$ is a constant characteristic of the process.

If we now consider a segment in the channel of a transistor at location y and of length dy as depicted in Fig. 9, it follows from (45) and the notation of Fig. 11 that the charge density can be expressed as

$$Q(y) = C_{ox}(V_{GS} - V_T - V(y)) \tag{53}$$

If the port variables are assured fixed, it follows from (53) that

$$\sigma^2(Q(y)) = C_{ox}^2 \sigma^2(V_T) \tag{54}$$

and from (52) that

$$\sigma^2(Q(y)) = C_{ox}^2 \frac{\tilde{A}_{VT}^2}{A} \tag{55}$$

If V_T in (45) is assured to be stochastic, it can be expressed as

$$V_T = V_{TN} + V_{TR} \tag{56}$$

where V_{TN} is the nominal value of the threshold voltage and V_{TR} is the random component of the threshold voltage. It thus follows that (46) can be expressed as

$$I_D dy = \mu C_{OX} W (V_{GS} - V_{TN} - V_{TR} - V(y)) dV(y) \tag{57}$$

If this is now integrated from the drain to source of the segmented transistor, we obtain

$$I_D = \frac{\mu C_{OX} W}{dy} (V_{GS} - V_{TN} - \frac{V(y+dy) - V(y)}{2})(V(y+dy) - V(y)) + \frac{\mu C_{OX} W}{dy} \int_{V(y)}^{V(y+dy)} V_{TR} dV(y) \tag{58}$$

If we now assume that

$$\int_{V(y)}^{V(y+dy)} V_{TR} dV(y) = \left[\int_{A\_Segment} V_{TR}(x, y) dx dy \right] (V(y+dy) - V(y)) \tag{59}$$

then I_D can be expressed as

$$I_D = \frac{\mu C_{OX} W}{dy} (V_{GS} - V_{TM} - \frac{V(y+dy) - V(y)}{2})(V(y+dy) - V(y)) \tag{60}$$

where the model threshold voltage, V_{TM}, satisfies the relation

$$V_{TM} = V_{TN} + \left[\int_{A\_Segment} V_{TR}(x, y) dx dy \right] \tag{61}$$

This is the standard square law model for the segmented transistor. It follows from (60) that

$$\sigma^2(I_D) = (\frac{\mu C_{OX} W}{dy})^2 (V(y+dy) - V(y))^2 \sigma^2(V_{TM}) \tag{62}$$

but from (44) and (54) that

$$\sigma^2(I_D) = (\frac{\mu C_{OX} W}{dy})^2 (dV(y))^2 \sigma^2(V_T) \tag{63}$$

From (62) and (63), it thus follows that

$$\sigma^2(V_{TM}) = \sigma^2(V_T) \tag{64}$$

It can be shown that the expected values of V_T and V_{TM} also agree for the segmented

transistor. The model of the threshold voltage of (63) was used for the simulations that were summarized in Fig. 10 and this resulted in an inconsistent model. It should be noted that the relationship of (63) is a direct consequence of the relationship of (54) which was obtained since the port variables in the segment model were assumed fixed.

It should be observed, however, that in an actual transistor, the charge density is strongly dependent upon the position in he channel. Equation (54) obtained under the assumption that the port voltages are not stochastic, indicates that the variance in the channel charge density is independent of position since the statistics of the process threshold voltages are independent of position. However, it can be observed from (45) and (50) that

$$Q(y) = C_{ox}(V_{GS}-V_T)\sqrt{1-\frac{y}{L}} \tag{65}$$

Thus

$$\sigma^2(Q(y)) = C_{ox}^2(1-\frac{y}{L})\sigma^2(V_T) \tag{66}$$

or, equivalently from (50)

$$\sigma^2(Q(y)) = C_{ox}^2(1-\frac{V(y)}{V_{GS}-V_T})^2\sigma^2(V_T) \tag{67}$$

Note that (66) differs considerably from (54) obtained under the assumption that the port variables were non-stochastic. It follows from (44) and (66) that

$$\sigma^2(I_D) = \frac{\mu^2 C_{ox}^2 W^2(1-\frac{y}{L})}{(dy)^2}\sigma^2(V_T) \tag{68}$$

Thus from (62) and (68), we obtain

$$\sigma^2(V_{TM}) = (1-\frac{y}{L})\sigma^2(V_T) \tag{69}$$

and thus from (52) that

$$\sigma^2(V_{TM}) = (1-\frac{y}{L})\frac{\tilde{A}_{VT}^2}{A} \tag{70}$$

or, equivalently

$$\sigma^2(V_{TM}) = (1-\frac{V(y)}{V_{GS}-V_T})\frac{\tilde{A}_{VT}^2}{A} \tag{71}$$

Equations (66) and (67) are equivalent when the device is operating in the saturation region. If the transistor is operating in the triode region, (50) no longer applies but it can be shown that (67) and correspondingly (71) remain valid.

From (64) and (69), it is apparent that the probability density function of the model parameter, V_{TM}, differs from that of the process parameter V_T and this difference is very significant as the saturated part of the channel is approached.

The model of (70) was used to model the stochastic threshold voltage for the segmented transistors in HSpice. The simulation results for the drain current standard deviation of a single transistor are shown in Fig. 12 for the same test condition used in the previous section.

It can be seen that the results now converge. The issue of what value of variance actually characterizes the device must be addressed since the variance is dependent upon the number of segments used in the simulation. The value is the asymtotic value shown in the figure. If a small number of segments are used, the channel voltage dependence on V_{TM} is quantified into a small number of bins and this quantization biases the simulation results.

Also shown in the figure are the simulation results for a transistor operating in the triode region biased at V_{GS}=2.5V, V_{DS}=1V, and V_{TN}=0.8V. It can be observed that it

converges to the same value as was obtained for the saturated channel device, This indicates that the normalized variance in the drain current is not operation region dependent. If, however, a single-segment model is used, it can be shown analytically that the statistics for I_D are strongly operating point dependent and vary considerably between the triode and saturation regions. This can be seen as well in the plot of Fig. 12 in the case where N=1.

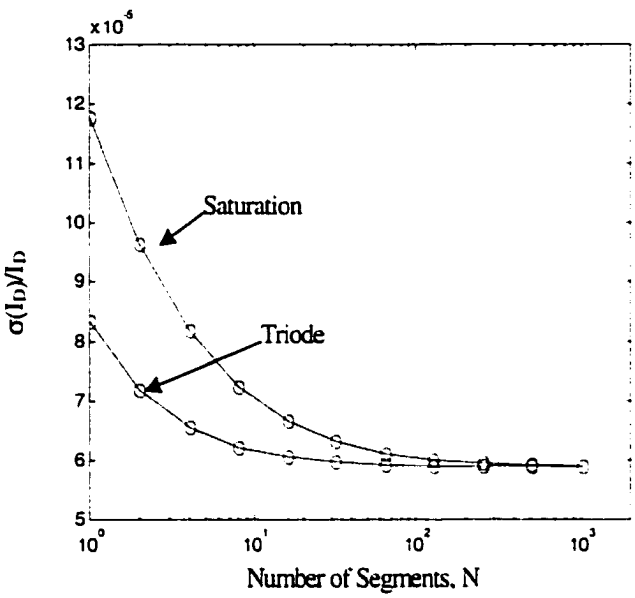

Fig. 12 Current mismatch for a single device operating in saturation and triode regions with the model of (71)

The issue of consistency in the variance model of (66) and (71) also deserves consideration. Simulations of two series connected transistors have been made and the results show convergence to the same values as was obtained for the single equivalent transistor indicating that the model is consistent.

Unfortunately, the time required for a Spice-type simulation needed to obtain convergence is very long because of the large number of segments needed and because of the large number of simulations needed for each value of N. An alternative development that

circumvents the need for the large number of Spice simulation will now be developed.

According to graduation channel approximation, drain current can be expressed as

$$I_D = \frac{\int_{V=0}^{V=V_D} Q(y)W\mu_n dV}{\int_{y=0}^{y=L} dy}$$
$$= \frac{\int_0^{V_1} Q_0(y)W\mu_n dV + \int_{V_1}^{V_2} Q_1(y)W\mu_n dV + \ldots + \int_{V_i}^{V_{i+1}} Q_i(y)W\mu_n dV + \ldots + \int_{V_{N-1}}^{V_D} Q_{N-1}(y)W\mu_n dV}{\int_{y=0}^{y=L} dy} \quad (72)$$
$$= \frac{\sum_{i=0}^{N-1}\int_{V_i}^{V_{i+1}} Q_i(y)W\mu_n dV}{\int_{y=0}^{y=L} dy}$$

where N=L/dy, V_0=0, and V_{N-1}=V_D. If there is a variation happening to charge density, then $Q_i(y)$ can be expressed as $Q_{i\_Nom}(y)+Q_{i\_Rand}(y)$ where $Q_{i\_Nom}(y)$ and $Q_{i\_Rand}(y)$ are the nominal charge density and its variation at the position y respectively. Thus (72) can be rewritten as

$$I_D = \frac{\sum_{i=0}^{N-1}\int_{V_i}^{V_{i+1}} (Q_{i\_Nom}(y)+Q_{i\_Rand}(y))W\mu_n dV}{\int_{y=0}^{y=L} dy}$$
$$= \frac{\sum_{i=0}^{N-1}\int_{V_i}^{V_{i+1}} Q_{i\_Nom}(y)W\mu_n dV + \sum_{i=0}^{N-1}\int_{V_i}^{V_{i+1}} Q_{i\_Rand}(y)W\mu_n dV}{\int_{y=0}^{y=L} dy} \quad (73)$$
$$= \frac{\sum_{i=0}^{N-1}\int_{V_i}^{V_{i+1}} Q_{i\_Nom}(y)W\mu_n dV}{\int_{y=0}^{y=L} dy} + \frac{\sum_{i=0}^{N-1}\int_{V_i}^{V_{i+1}} Q_{i\_Rand}(y)W\mu_n dV}{\int_{y=0}^{y=L} dy} = I_{D\_Nom} + \frac{\sum_{i=0}^{N-1}\int_{V_i}^{V_{i+1}} Q_{i\_Rand}(y)W\mu_n dV}{\int_{y=0}^{y=L} dy}$$

where I_{D_Nom} is defined as the nominal current through the device. Thus the variation happens to the current through the device due to charge density variation can be expressed as

$$\frac{I_D - I_{D\_Nom}}{I_{D\_Nom}} = \frac{\sum_{i=0}^{N-1}\int_{V_i}^{V_{i+1}} Q_{i\_Rand}(y)W\mu_n dV}{\sum_{i=0}^{N-1}\int_{V_i}^{V_{i+1}} Q_{i\_Nom}(y)W\mu_n dV} = \sum_{i=0}^{N-1}\left(\frac{\int_{V_i}^{V_{i+1}} Q_{i\_Rand}(y)W\mu_n dV}{\int_{V_i}^{V_{i+1}} Q_{i\_Nom}(y)W\mu_n dV}\frac{\int_{V_i}^{V_{i+1}} Q_{i\_Nom}(y)W\mu_n dV}{\sum_{i=0}^{N-1}\int_{V_i}^{V_{i+1}} Q_{i\_Nom}(y)W\mu_n dV}\right) \quad (74)$$

Also, the conductance in the ith region can be approximated as

$$C_i(y)=\frac{\int_{V_i}^{V_{i+1}} Q_i(y)W\mu_n dV}{dL(V_{i+1}-V_i)}=\frac{\int_{V_i}^{V_{i+1}} (Q_{i\_Nom}(y)+Q_{i\_Rand}(y))W\mu_n dV}{dL(V_{i+1}-V_i)} \tag{75}$$
$$=\frac{\int_{V_i}^{V_{i+1}} Q_{i\_Nom}(y)W\mu_n dV}{dL(V_{i+1}-V_i)}+\frac{\int_{V_i}^{V_{i+1}} Q_{i\_Rand}(y)W\mu_n dV}{dL(V_{i+1}-V_i)}$$

Thus the conductance in the ith region can be expressed as $C_{i\_Nom}(y)+C_{i\_Rand}(y)$ where $C_{i\_Nom}(y)$ and $C_{i\_Rand}(y)$ are given by

$$C_{i\_Nom}(y)=\frac{\int_{V_i}^{V_{i+1}} Q_{i\_Nom}(y)W\mu_n dV}{dL(V_{i+1}-V_i)} \tag{76}$$

$$C_{i\_Rand}(y)=\frac{\int_{V_i}^{V_{i+1}} Q_{i\_Rand}(y)W\mu_n dV}{dL(V_{i+1}-V_i)} \tag{77}$$

The equation (74) can thus be expressed as

$$\frac{I_D-I_{D\_Nom}}{I_{D\_Nom}}=\sum_{i=0}^{N-1}\left(\frac{C_{i\_Rand}(y)}{C_{i\_Nom}(y)}\frac{\int_{V_i}^{V_{i+1}} Q_{i\_Nom}(y)W\mu_n dV}{\sum_{i=0}^{N-1}\int_{V_i}^{V_{i+1}} Q_{i\_Nom}(y)W\mu_n dV}\right) \tag{78}$$

The term in the above equation (78) can be simplified as

$$\int_{V_i}^{V_{i+1}} Q_{i\_Nom}(y)W\mu_n dV=C_{OX}W\mu_n\left((V_{GS}-V_{TN})(V_{i+1}-V_i)-\frac{1}{2}(V_{i+1}^2-V_i^2)\right) \tag{79}$$

where V_{i+1} and V_i can be expressed as

$$V_{i+1}=(V_{GS}-V_{TN})\left(1-\sqrt{1-\frac{y_{i+1}}{L}}\right) \tag{80}$$

$$V_i=(V_{GS}-V_{TN})\left(1-\sqrt{1-\frac{y_i}{L}}\right) \tag{81}$$

where $y_i=(i/N)L$.

Substituting (80) and (81) into (79) and then the following equation will be given

$$\int_{V_i}^{V_{i+1}} Q_{i\_Nom}(y) W\mu_n dV = C_{OX} W\mu_n (V_{GS} - V_{TN})^2 (\frac{y_{i+1} - y_i}{2L}) = C_{OX} W\mu_n (V_{GS} - V_{TN})^2 (\frac{1}{2N}) \quad (82)$$

Substituting (82) into (78) and the following expression will be given

$$\frac{I_D - I_{D\_Nom}}{I_{D\_Nom}} = \sum_{i=0}^{N-1} (\frac{C_{i\_Rand}(y)}{C_{i\_Nom}(y)} \frac{\int_{V_i}^{V_{i+1}} Q_{i\_Nom}(y) W\mu_n dV}{\sum_{i=0}^{N-1} \int_{V_i}^{V_{i+1}} Q_{i\_Nom}(y) W\mu_n dV}) \quad (83)$$

$$= \sum_{i=0}^{N-1} (\frac{C_{i\_Rand}(y)}{C_{i\_Nom}(y)} \frac{(V_{GS} - V_{TN})^2 (\frac{1}{2N})}{\sum_{i=0}^{N-1} (V_{GS} - V_{TN})^2 (\frac{1}{2N})}) = \frac{1}{N} \sum_{i=0}^{N-1} \frac{C_{i\_Rand}(y)}{C_{i\_Nom}(y)}$$

Thus the variation of current through the device can be represented as

$$\frac{\sigma^2(I_D)}{I_{D\_Nom}^2} = (\frac{1}{N})^2 \sum_{i=0}^{N-1} \frac{\sigma^2(C_i(y))}{C_{i\_Nom}^2(y)} \quad (84)$$

where $\sigma(C_i(y))$ is readily derived from (43) as

$$\sigma^2(C(y)) = \mu^2 C_{OX}^2 \frac{W^2}{dy^2} (1 - \frac{y}{L}) \sigma_v^2(V_T) \quad (85)$$

and C_{i_Nom} can be simply derived from the gradual channel approximation. The drain current, $I_{D,yi}$, through the region in Fig. 11b can be given by

$$I_{D,yi} = \mu C_{OX} \frac{W}{dy} ((V_G - V(y_i) - V_{TN}) dV(y_i) - \frac{1}{2} dV(y_i)^2) \quad (86)$$

where $dV(y_i)=V(y_{i+1})-V(y_i)$. Thus, the conductance of the region, dy, can be given by

$$C_i(y) = \frac{I_{D,y}}{dV(y_i)} = \mu C_{OX} \frac{W}{dy} ((V_G - V(y_i) - V_{TN}) - \frac{1}{2} dV(y_i)) \quad (87)$$

Substituting (85) and (87) into (84), the current variation can be expressed as

$$\frac{\sigma^2(I_D)}{I_{D\_Nom}^2} = (\frac{1}{N})^2 \sum_{i=0}^{N-1} \frac{\sigma_i^2(V_T)(1 - \frac{y_i}{L})}{(V_G - V(y_i) - V_{TN} - \frac{1}{2} dV(y_i))^2} \quad (88)$$

where $\sigma_i(V_T)$ is the V_T variation happening within *i*th region of length dy and width W.

However, when N approaches to the infinity, $dV(y_i)$ will approach zero and thus (88) can be simplified as

$$\frac{\sigma^2(I_D)}{I^2_{D\_Nom}} = (\frac{1}{N})^2 \sum_{i=0}^{N-1} \frac{\sigma_i^2(V_T)(\frac{V_{GS}-V_{TN}-V(y_i s)}{V_{GS}-V_{TN}})^2}{(V_G - V(y_i) - V_{TN})^2} = (\frac{1}{N})^2 \sum_{i=0}^{N-1} \frac{\sigma_i^2(V_T)}{(V_{GS}-V_{TN})^2} \tag{89}$$

Although there is an assumption of operating in saturation region, $V_{DS}=V_{GS}-V_T$, in the beginning, (88) and (89) can also be proven valid within the triode region and $V(ys)=V(y)-V_S$ can be expressed as

$$V(ys) = (V_{GS}-V_T) - \sqrt{(V_{GS}-V_T)^2 - \frac{2y}{L}((V_{GS}-V_T)V_{DS} - \frac{1}{2}V_{DS}^2)} \tag{90}$$

These current variation models, (88) and (89), are derived under an assumption of a single device and thus the current variation for a pair of current mirror can be expressed by

$$\frac{\sigma^2(\Delta I_D)}{I^2_{D\_Nom}} = \frac{2\sigma^2(I_D)}{I^2_{D\_Nom}} = 2(\frac{1}{N})^2 \sum_{i=0}^{N-1} \frac{\sigma_i^2(V_T)(1-\frac{V(y_i s)}{V_{GS}-V_{TN}})^2}{(V_G - V(y_i) - V_{TN} - \frac{1}{2}dV(y_i))^2} \tag{91}$$

$$\frac{\sigma^2(\Delta I_D)}{I^2_{D\_Nom}} = \frac{2\sigma^2(I_D)}{I^2_{D\_Nom}} = 2(\frac{1}{N})^2 \sum_{i=0}^{N-1} \frac{\sigma_i^2(V_T)}{(V_{GS}-V_{TN})^2} \tag{92}$$

Next, the validity and consistency of model (88) and (89) are going to be verified. The device used for the verification is assumed with the size of width 100μm and length 100μm and will be simulated under two working regions. One is working in the saturation region, $V_{DS}=V_{GS}-V_T$, where $V_D=1.7V$, $V_G=2.5V$, $V_S=0$, and $V_T=0.8V$, and the other is the triode region where $V_D=1V$, $V_G=2.5V$, $V_S=0$, and $V_T=0.8V$. Similarly, the device is partitioned into N segments and is shown in Fig. 9b. The simulation model is a level 2 device model for 2μm n-well process available through MOSIS except that V_T is replaced by 0.8V and $\tilde{A}_{VT}$ is

assumed as 10mV·μm. The simulation results of (88) with two working regions are plotted as a function of the number of segments, N, in Fig. 13. The results show there is an excellent agreement between Hspice and Matlab simulation results.

Then, we are going to consider another model (89). Because the device is rectangular, the simulation with the approach (89) will be simple and can be expressed as

$$\frac{\sigma^2(I_D)}{I_{D\_Nom}^2} = \frac{\sigma_i^2(V_T)}{N(V_{GS} - V_{TN})^2} = \frac{\tilde{A}_{VT}^2}{WL(V_{GS} - V_{TN})^2} \tag{93}$$

(93) can be easily simulated by Matlab and the simulation results are also plotted in Fig. 13. From the Fig. 13, it is apparent that the simulation results with (89) are independent of the number of segments, N, and the results of the approach (88) will converge when N becomes larger. Also, all curves are essentially coincident for large N. It is also shown in Fig. 13 that the current variations, $\sigma(I_D)/I_{D\_Nom}$, within saturation and triode regions have the same asymptotic value with given V_{GS} and V_T although they have different starting points (when N=1).

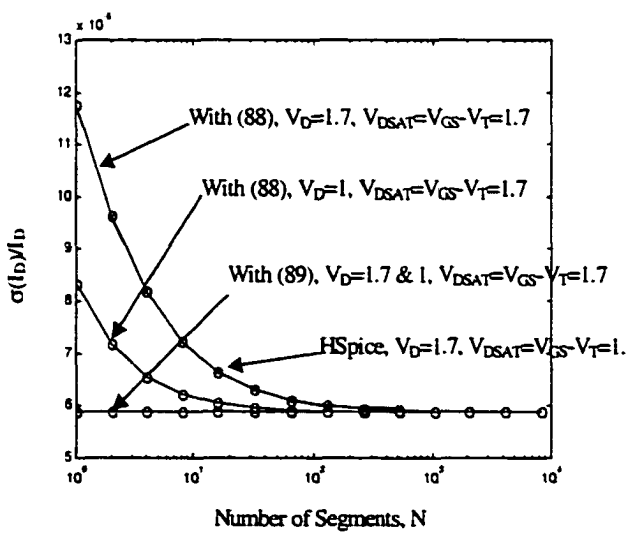

Fig. 13 Current mismatch for a single device using Matlab and Hspice

VII. Effects of Random Parameter Variations on Matching

Equation (88) with N=1 (y=0) is rewritten as

$$\frac{\sigma^2(I_D)}{I_{D\_Nom}^2} = \frac{\sigma^2(V_T)}{(V_{GS} - V_{TN} - \frac{1}{2}(V_{DS}))^2} \tag{94}$$

Then $V_{DS}=V_{GS}-V_{TN}$ is substituted into (94) and then the following equation will be given

$$\frac{\sigma^2(I_D)}{I_{D\_Nom}^2} = \frac{4\sigma^2(V_T)}{(V_{GS} - V_{TN})^2} \tag{95}$$

In the traditional approach to modeling random parameters, $\sigma(V_T)$ in (94) and (95) can be expressed as

$$\sigma^2(V_T) = \frac{A_{VT}^2}{WL} \tag{96}$$

The two equations, (94) and (95), have been widely used to extract model parameters in the triode and saturation regions respectively and these equations are the same as (39) and (40). According to the simulation results shown in Fig. 13 for (88) and (89), it shows that the current variation, $\sigma(I_D)/I_D$, will be a constant with a given excess voltage within the range, $0 \le V_D \le V_{GS}-V_T$. This implies that the extracted area proportionality constant, A_{VT}, will be V_{DS} dependent according to (94) and (95) with a given excess voltage. If current mismatch can be measured and threshold voltage statistics can be inferred from (94) and (95), the measurements will inherently be made on a distributed device and be the asymptotic values depicted in Fig. 13. Thus, the parameter A_{VT}'s for the equations (94) and (95) that give values that agrees with the measured results is what we need. Then the relationship between $\tilde{A}_{VT}$ and A_{VT} can be derived from (93) and (94) in the triode region as

$$\frac{\sigma^2(I_D)}{I^2_{D\_Nom}} = \frac{\tilde{A}^2_{VT}}{WL(V_{GS}-V_{TN})^2} = \frac{A^2_{VT}}{WL(V_G - V_S - V_{TN} - \frac{1}{2}(V_D - V_S))^2} \tag{97}$$

Thus the A_{VT} can be expressed in the term of $\tilde{A}_{VT}$ as

$$A_{VT} = (1 - \frac{1}{2}\frac{V_{DS}}{V_{GS} - V_{TN}})\tilde{A}_{VT} \tag{98}$$

The equation (98) is only valid within the range that the gradual channel approximation can be validly applied. After the device reaches to the deep saturation region, a depleted channel section ΔL will be introduced as shown in Fig. 14 and there is almost carrier free within this section. The depletion region, ΔL, can be derived by the first-order approximation as

$$\Delta L = \frac{\lambda(V_{DS} - V_{DSAT})L}{1 + \lambda(V_{DS} - V_{DSAT})} \tag{99}$$

where λ is called the channel length modulation parameter and $V_{DSAT}=V_{GS}-V_T$ is the pinch-off voltage.

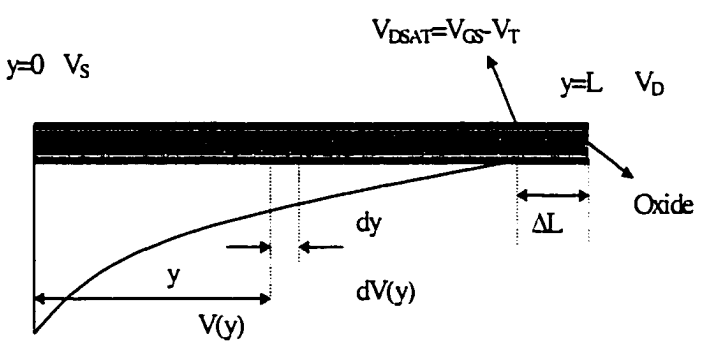

Fig. 14 Cross section of a device in saturation region

Because it is almost carrier free within the depletion region, the depletion region contributes nothing to current variation. Thus current variation in the deep saturation region can be expressed as

$$\frac{\sigma^2(I_D)}{I_{D\_Nom}^2} = \frac{\tilde{A}_{VT}^2}{WL(V_{GS} - V_{TN})^2}(1 - \frac{\Delta L}{L}) \tag{100}$$

Substituting (99) into (100) and the following expression will be given

$$\frac{\sigma^2(I_D)}{I_{D\_Nom}^2} = \frac{\tilde{A}_{VT}^2}{WL(V_{GS} - V_{TN})^2}\frac{1}{1 + \lambda(V_{DS} - V_{DSAT})} \tag{101}$$

According to (95) and (101), the relationship of A_{VT} and $\tilde{A}_{VT}$ in the deep saturation region can be given as

$$A_{VT} = \frac{\tilde{A}_{VT}}{2}\sqrt{\frac{1}{1 + \lambda(V_{DS} - V_{DSAT})}} \tag{102}$$

$A_{VT}/\tilde{A}_{VT}$ for (98) and (102) are plotted in Fig. 15 as a function of V_{DS}/V_{DSAT}, and $\tilde{A}_{VT}$, V_{DAST}, and λ are assumed as 10mV·μm, 1.7V, and $0.05V^{-1}$ respectively. In Fig. 15, it shows that there is a linear relationship existing between A_{VT} and $\tilde{A}_{VT}$ and after the device is going into the saturation region, the ratio of $A_{VT}/\tilde{A}_{VT}$ is almost constant. Unfortunately, this observation is easy to be ignored during the testing process.

VIII. Conclusion

The inherent error with the integral has been pointed out in this paper. The error is acceptable in a general application, but it is significant in the high-end circuits. For the systematic mismatch, this paper has given an overall view on how the prediction of the

matching performance of a layout can be skewed by the integral model. Also, it has been shown that there is an essential limitation with common centroid layouts and their matching performance is gradient angle dependant. For random mismatch, a new model for characterizing the effects of random variation of model parameters in MOS transistors has been introduced. This model overcomes the inconsistencies inherent in existing approaches for predicting the matching characteristics of devices and matching-critical circuits. The new model can be used to have a more accurate matching prediction of circuit performance and help researchers to extract the true area proportionality constants. The determination of true area proportionality constants will help to explain some unexpected observations related to random mismatch measurements.

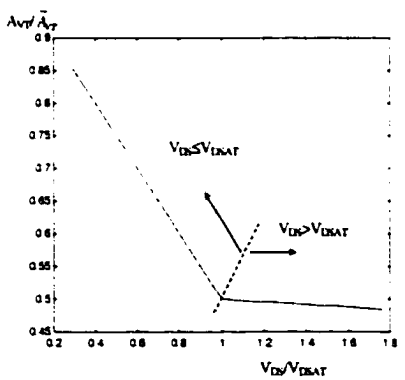

Fig. 15 $A_{VT}/\tilde{A}_{VT}$ in the function of V_{DS}/V_{DSAT}

Acknowledgements

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CHAPTER 3. A SIMULATOR FOR MATCHING-CRITICAL CIRCUITS WITH DISTRIBUTED CHANNEL PARAMETERS

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Abstract

A CAD tool, MOSGRAD, that can be used to simulate the effects of distributed two-dimensional systematic and random variations in device parameters on the performance of matching-critical circuits has been developed. This tool has been used to predict the effects of systematic and random parameter variations on the performance of current mirrors. It has also been used for predicting the performance of non-conventional circuit structures in which multiple drain and/or source regions share a common channel region and predicting the performance of non-conventional layouts that may incorporate nonrectangular transistors or multiply-segmented transistors.

I. Introduction

Iteration with device sizes and layout styles at the silicon level can improve performance but such an approach will not yield optimal designs and is both costly and time consuming. The preferred route for optimizing the design and layout is based upon simulation. The seemingly simple problem of predicting the effects of systematic and random variations on a MOS transistor is becoming complicated by the unavailability of a suitable simulator and by some inconsistencies on modeling [1]. Existing models and simulators provide little insight into how to change either the size or layout to improve performance.

The major reason existing simulators can not be used is that there is no mechanism for incorporating either systematic or random channel variations in lateral directions of device or process parameters. These lateral variations play a key role in the performance of high-end matching-critical circuits. Although process simulators are an appropriate tool for simulating the effects of parameter gradients, existing process simulators are limited to two dimensional modeling and only one of these dimensions is lateral. Correspondingly, the literature that relates to modeling transistors with non-uniform threshold voltages throughout the channel region depends upon the unjustifiable assumption that the equivalent threshold voltage of a transistor can be obtained by an area integral of the position dependent threshold voltage over the channel region [2]. Although this latter approach may provide a good approximation in some applications, it is inadequate for accurately predicting matching performance of current mirrors and differential amplifiers and leads to the incorrect conclusion that linear systematic gradients in process parameters are canceled in common centroid layout schemes [3].

In this paper, a CAD tool named as MOSGRAD that is capable of simulating the lateral variations has been developed and thus this tool can be used to predict the effects of systematic and random parameter variations on the performance of current mirrors more accurately.

II. Parameter Variations

It is well recognized that the matching performance of basic circuit elements is attributable to both systematic and random variations in geometric parameters, process parameters and device parameters. In the beginning of this section, we would like to give

clear definitions about the systematic and random variation factors. A process parameter P in a distributed device can be represented by the expression

$$P(x,y) = P_{NOM} + P_{PROC} + P_{WAFER} + P_{DIE} + P_{SYS}(x,y) + P_{RAN}(x,y) \quad (1)$$

where x and y represent the position on the die. In (1), P_{NOM} is the nominal value of the parameter P and the five remaining terms are themselves random variables that some authors choose to combine together into a single random variable. The variable P_{PROC} characterizes the variation of the parameter P from one lot of wafers to another. The parameter P_{WAFER} characterizes the variation of P from one wafer to another wafer in a "lot" of wafers and the parameter, P_{DIE}, characterizes the variation of the parameter from die location to die location. The parameter P_{SYS} characterizes the systematic variation of the parameter from one location to another on the die and is position dependent. The variable P_{RAN} characterizes the random part of the parameter at the position (x,y). When considering devices in close proximity to each other on a die, the values of the random variables P_{PROC}, P_{WAFER} and P_{DIE} are nearly constant throughout the region. Thus, almost all the matching-related research focus only on the effects of the two rightmost terms, P_{SYS} and P_{RAN}, in (1).

For using a Spice-type simulator, the performance of a device is characterized by a set of model parameters. The model parameters for a MOSFET include the threshold voltage (V_T), the mobility (μ), the gate oxide capacitance density (Cox), etc. Some of these model parameters are determined from well-known relationships between the process parameters and others are more empirical in nature. Since the process parameters are position dependent, the model parameters are position dependent as well and thus since the underlying process parameters are stochastic, the model parameters are stochastic. Although many of the process parameters are uncorrelated or weakly correlated, a single process parameter often affects

more than one model parameter causing correlation between the model parameters. This correlation is often neglected when characterizing the matching characteristics of linear circuits. Following this standard approach for characterizing the process parameters, the device model parameters can be expressed in the form

$$\gamma(x,y)=\gamma_{NOM}+\gamma_{PROC}+\gamma_{WAFER}+\gamma_{DIE}+\gamma_{SYS}(x,y)+\gamma_{RAN}(x,y) \quad (2)$$

where γ represents the model parameters.

III. Existing Approaches on Variation Modeling

Implicit in the functional form of (2) is the distributed nature of the model parameter. Essentially all device models and, in particular, the device models used in Spice-type simulators are based upon lumped parameter models. In most works, it is assumed that the actual values of the lumped model parameters can be obtained by integrating the position-dependent distributed model parameters over the area of the channel region of the device as given by the equation.

$$\gamma(x_A, y_A) = \frac{1}{\text{Area}} \iint_{\text{Area}} \gamma(x, y)\,dx\,dy \quad (3)$$

where (x_A,y_A) is a point representation of the location of the device on the die [3-5]. Although not critical in what follows, it is convenient to define (x_A,y_A) to be the geometrical centroid of the device. We will refer to this lumped parameter extraction from a distributed parameter domain as the integral model through this paper. This approach of mapping from a distributed stochastic parameter to a single lumped model parameter has been used almost exclusively for well over a decade and the issue of validity of this mapping is generally not questioned. Unfortunately, the discrepancies and limitations with the mismatch models based

upon the integral model have been reported and observed in the papers [1][5][6]. Although the paper [6] has proposed a new approach to improve the modeling on mismatch, however the proposed approach is still based on the integral model and thus the inherent limitation [1][5] with the integral model still exists. Since both systematic effects and random fluctuations in device parameters are important roles in matching performance, it is particularly important that an adequate approach on mismatch modeling should be able to sufficiently and effectively incorporate these fluctuations. Moreover, when the integral model (3) is applied to a device of non-conventional shape, sometimes, it is very hard to find a close-form formula to model mismatch performance and even express the I/V characteristics. Although there is a report about modeling non-rectangular device [7], the approach still has a limitation to derive a close-form formula with an arbitrary-shape device. Thus, an alternative approach for predicting mismatch performance of matching-critical circuits will be proposed. This approach can be used to predict the matching characteristics of an arbitrary layout of any size for arbitrary gradients in threshold voltage or any other process parameters and as such, can be used to overcome the errors inherent with the integral model.

IV. Proposed Approach

The approach we propose for predicting the matching performance is based upon the finite-element approach. Time consuming and memory requirements are the major drawbacks of the finite-element approach. Fortunately, these drawbacks can be overcome easily by the advance of technology in computers for the past few years.

This approach approximates the distributed channel region by an assemblage of finite lumped-element cells. Each cell has four edge-centered nodes that can be connected to

corresponding edge-centered nodes in adjacent cells as depicted in Fig. 1. One cell in Fig. 1 is expanded into Fig. 2. If the cell is assumed length L and width W, the size of MC1 and MC2 will be W/(L/2) and the size of MC3 and MC4 (W/2)/L. The four transistors in a unit cell will have a common gate terminal. With this finite lumped-element approach, systematic variations in process or device parameters of any magnitude and at any angle relative to the cell can be readily simulated using a conventional Spice-type simulator. Arbitrary systematic parameter variations and random parameter variations can also be accommodated. Although random mismatch is theoretically suitable with this finite-element approach, the simulation time and memory requirements are not trivial in practical. Thus, we have an alternate way to predict the random mismatch and it will be introduce in the later section.

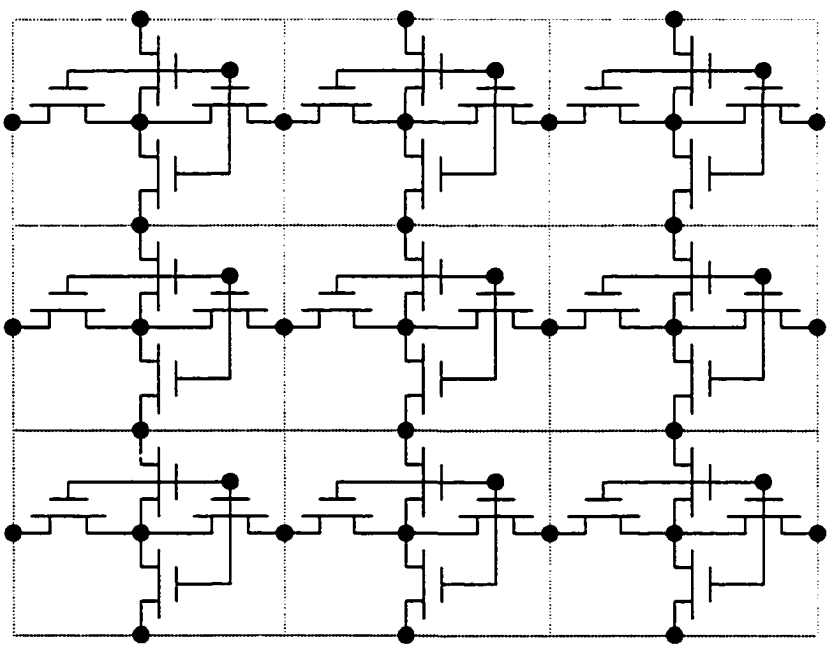


Fig. 1 Finite lumped-element model of 4-transistor cells

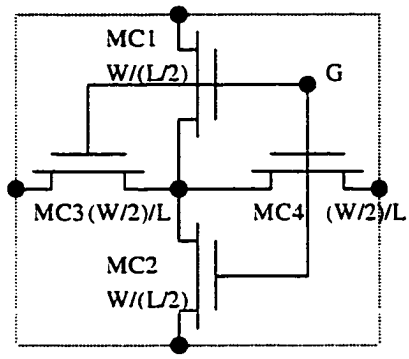


Fig. 2 Unit cell of 4-transistor

As a front end to the tool, a graphical users interface is incorporated in which the user graphically enters the circuit structure that is to be simulated. The graphical users interface is written by Matlab because that it has powerful and friendly functions to deal with graphical interaction. The output of the graphical interface is a file to record the information about the device shape and then the file will be sent to next simulation step, Netlist-Genetator. The core of Netlist-Generator is written by C language and its main function is to accommodate systematic parameter variations. The output from Netlist-Generator is a lumped-element circuit that is passed to a conventional Spice simulator. This tool is specifically focused towards predicting the performance of current mirrors and differential amplifiers in the presence of arbitrary threshold voltage gradients that occur at any angle across a die. Although the tool was established for predicting circuit performance under linear gradients, arbitrary gradients in process parameters can also be simulated. The graphical interface with Matlab allows the user to describe current mirrors or differential amplifiers comprised of arbitrarily shaped transistors. The results simulated by Spice will be summarized in the next

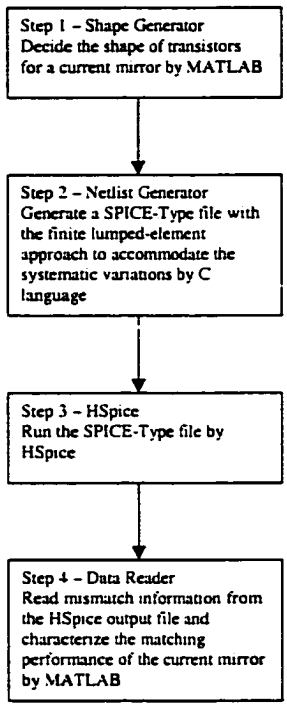


Fig. 3 Simulation diagram flow for systematic mismatch in MOSGRAD

step called data reader written by Matlab. The simulation procedure of this tool can be summarized into a simple diagram flow shown in Fig. 3.

V. Simulation Results on Systematic Mismatch

In this section, the effects of threshold voltage gradients on the matching performance of current mirrors will be investigated. A basic current mirror is depicted in Fig. 4. The input port is at the drain of transistor M1, the output is at the drain of transistor M2 and the sources are common. Three different layouts of a current mirror are shown in Fig. 5. In Fig. 5, α represents the magnitude of a parameter gradient and θ the angle of a parameter gradient. The contacts labeled as "D1" represent the drain contacts of M1 and the contacts labeled as

"D2" represent the drain contacts of M2. The mismatch of drain current is defined as $(I_{D2}-I_{D1})/I_{D1}$ when $V_{D1}=V_{D2}$. Because it is well known that the dominant factor of mismatch is the threshold voltage, we thus focus the discussion mainly on the parameter of threshold voltage. The effects of threshold voltage gradients at any angle across a die for interdigitized and common centroid layouts shown in Fig. 5b and 5c respectively are compared with the matching characteristics of a simple mirror layout shown in Fig. 5a. This comparison will be under the assumption of same area and drain current. The parameter gradients are modeled in a distributed way through the active devices themselves. The magnitude of the threshold gradient was assumed the same across each of the layouts and the angle of the gradient was varied continuously from 0° to 360° across the mirrors.

The matching characteristics of these current mirror layouts due to threshold voltage gradients are shown in Fig. 6 for a threshold gradient of 0.5mV/μm. These simulations are for NMOS current mirrors and with a Level 2 device model of 2 μm process available through MOSIS. The current mirrors in these simulations have the same total area size of 2048 μm^2 and W1, W2, and L in Fig. 5 are assumed as 32μm, 16μm and 32μm respectively. The results in Fig. 6 show that the matching characteristics are strongly a function of the angle of the threshold gradient across a die. Since the direction of the gradient in threshold voltage across a die may vary from one die lot to the next, this figure shows that measured results from test structures may not be good indicators of production performance. In addition to predicting the effects of an arbitrary gradient, this figure shows that a major improvement in mirror matching is achievable with the common centroid layout which is expanded in Fig. 7. For any angle, the effects of the threshold gradient for the common centroid layout is small. From Fig. 7, it is apparent that the common centroid structure has a

worst case matching error of 0.0035% for a threshold gradient of 0.5mV/u and this occurs at an angles of 45°, 135°, 225°, and 315°. In contrast to the well-accepted premise that the effects of linear gradients can be readily modeled [8] and are inherently canceled in common centroid structure [3], the threshold gradients through the devices themselves do create an angle-dependent gradient even in common centroid structures that assumes a maximum at every 45° angle through a simple common centroid layout.

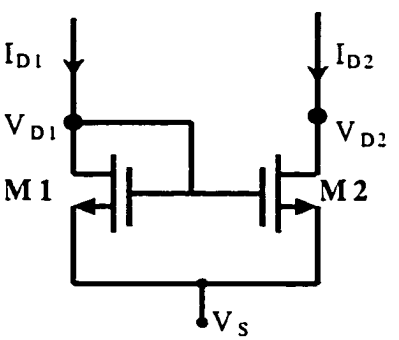
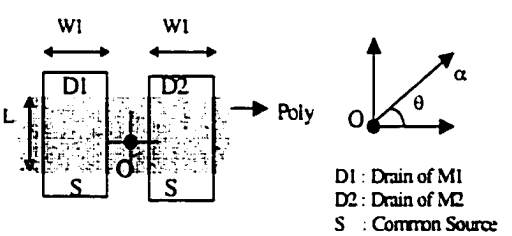
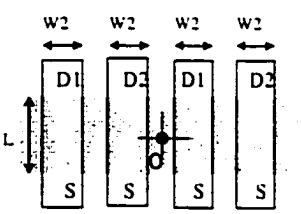


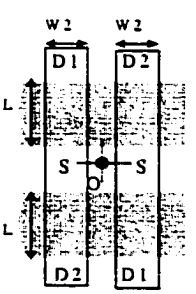
Fig. 4. Basic current mirror circuit



(a) Simple



(b) Interdigitized



(c) Common Centroid

Fig. 5 Current mirror layouts

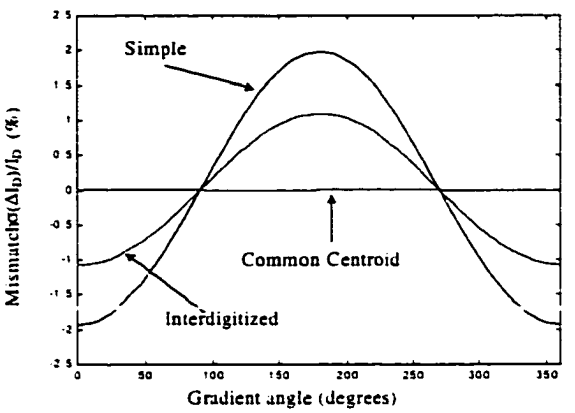


Fig. 6 Matching characteristics of the 3 mirror layouts

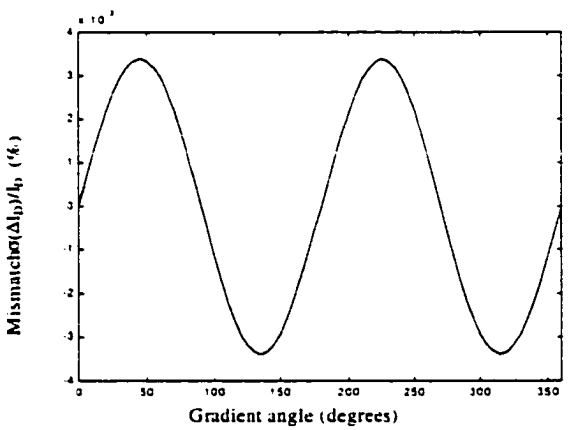


Fig. 7 Matching characteristics of common centroid layout

VI. Test Chip and Measurement Method

A test chip designed to verify the validity of the gradient matching prediction in MOSGRAD is shown in Fig. 8. The test circuit on this chip was a single simple current mirror using the simple layout, Fig. 5a. The width and length of each transistor were both identical (W1=L=32μm) and the spacing between the two transistors was 4μm. This chip has been fabricated in 2μm CMOS n-well process available through MOSIS. In the test structure,

the V_T gradient was controlled via the back bias on the transistors. P-channel transistors were placed in a large circular n-well. Multiple periphery contacts where placed around the entire periphery of this n-well region. Currents were then introduced at any predetermined angle by selecting the appropriate diagonally opposing well contacts. These currents introduced a gradient voltage in the well which correspondingly induced a gradient in the threshold voltage of the test transistors. For dimensions of the transistors that are reasonably small relative to the diameter of the n-well, the result of V_T gradient is quite linear. The magnitude of the well current is directly related to the magnitude of the induced threshold gradient. It can be shown that a 1.189mv/u gradient in the substrate at the location of the test device will create a threshold voltage gradient of approximately 0.322mv/u. To avoid forward biasing the well-diffusion junction, the substrate voltage around the test current mirror was kept at about 6V, while the drain and source diffusions were restricted to be at most 5V.

The measured results of mismatch on drain current will be the effect of mismatches of all parameters and they can be expressed as a function like

$$\frac{\Delta I_D}{I_D} = f(\Delta V_T, \Delta\mu, \Delta C_{OX}, \Delta L, \Delta W, etc.) \tag{4}$$

For our test chip, V_T gradient is deigned to be adjustable by controlling the substrate voltages and thus the V_T gradient is attributable to electrical-control gradient and native gradient. Then, the equation can be re-formulated as

$$\frac{\Delta I_D}{I_D} = f_1(\Delta V_{TE}) + f_2(\Delta V_{T,Native}, \Delta\mu, \Delta C_{OX}, \Delta L, \Delta W, etc.) \tag{5}$$

where ΔV_{TE} and $\Delta V_{T.Native}$ represent the electrically-controlled gradient and native gradient respectively. The second term shown in the equation (5) will be expected to "offset" the $(\Delta I_D/I_D)$ results.

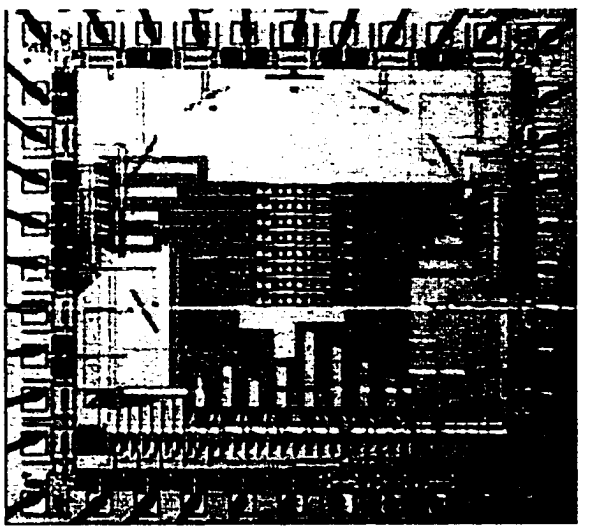


Fig. 8 The test chip of the simple structure

VII. Experiment Results

The test results of the simple structure, Fig. 5a, are shown in Fig. 9 and it is apparent that there is an offset existing. If the offset is filtered out, there is a good agreement between the measured and simulated results. The peak-to-peak variation of the measured result was about 1.55% and the peak-to-peak variation of the simulation was also about 1.56%. The upward shift is about 0.5% for the test structure compared to that of the simulation. As the mention in the previous section, the reason for this shift is due to the random mismatches in the test structure and the native gradient due to processing. In this test, a 1.189mv/u gradient in the substrate was applied at the location of the test device and it created a threshold voltage gradient of approximately 0.322mV/μm. Another testing results for the same simple structure, Fig. 5a, are shown in Fig. 10. This test is with a 0.734mV/μm gradient in the substrate at the location of the test device and it introduced a threshold voltage gradient of approximately 0.2mV/μm. The peak-to-peak variation of the measured result was about

0.96% and the peak-to-peak variation of the simulation was also about 0.96%. In addition, the other measured results for the interdigitized structure, Fig. 5b, are shown in Fig. 11. If the offset is filtered out, it also shows that there is a good agreement between the measured and simulated results. The testing results show that the simulator has successfully estimated the effect of the gradient threshold voltage in the performance of the current mirror. We believe the simulator effectively models the gradient effects in other structures as well.

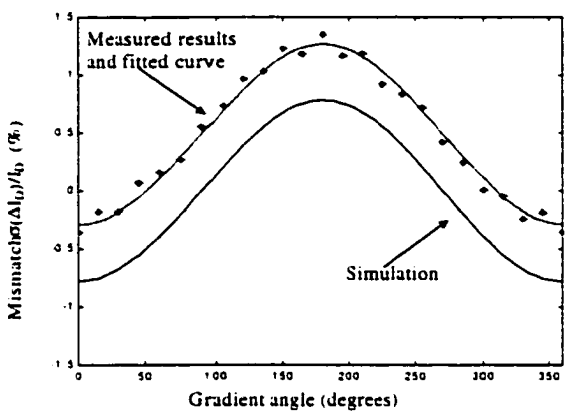


Fig. 9 Comparison between the experimental and simulation results of simple structure with V_T gradient of 0.322 mV/μm

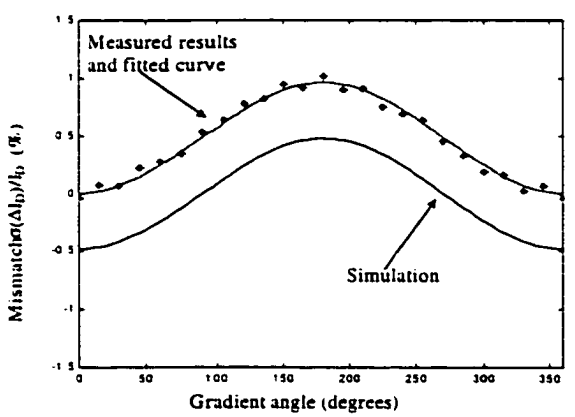


Fig. 10 Comparison between the experimental and simulation results of simple structure with V_T gradient of 0.2 mV/μm

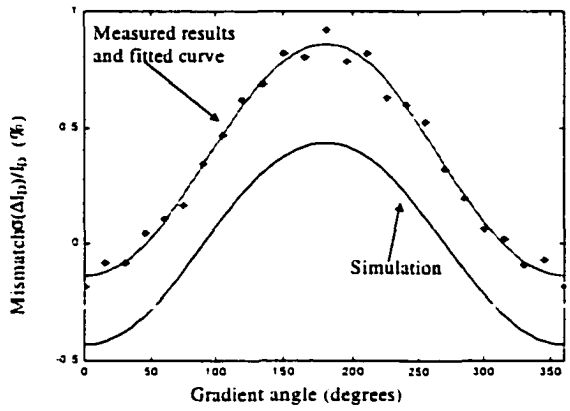


Fig. 11 Comparison between the experimental and simulation results of interdigitized structure with V_T gradient of 0.322 mV/μm

VIII. Simulation Results on Random Mismatch

Random mismatch also plays a key role in the matching performance of matching-critical circuits. It is commonly recognized that the random mismatch is inversely proportional to the active areas of matching circuits and this is often referred to as the "law of area" [2]. With the "law of area", the random mismatch of a model parameter, γ, can be expressed as

$$\sigma^2(\gamma) = \frac{A_\gamma^2}{\text{Area}} \tag{6}$$

where A_γ is the area proportionality constant. When $\sigma(\gamma)$ is plotted as a function of $1/\sqrt{Area}$, A_γ is equal to the slope. It should be noted that there is a possible confusion about the definition of the parameter A_γ. In this work, the parameter A_γ defines the variance of the model parameter of a single transistor of area W·L. Alternatively, the parameter $A_{\Delta\gamma}$ is used to characterize the difference in the model parameter of two devices, each of area W·L. At

this point, we have to notice that the information about $\sigma(\gamma)$ is extracted from the measured data based upon the lumped model with the integral approach and thus there is a discrepancy existing between the real area proportionality constant $\tilde{A}_\gamma$ and extracted A_γ. In fact, $\tilde{A}_\gamma$ is theoretically constant in the same process and is independent of the shape of a device. However, a current report [9] showed a discrepancy that there was a significant difference between A_γ's with different shapes. In this section, we will emphasize on how to predict the standard deviation of mismatch on the drain current for a current mirror, in particular, with non-conventional shapes.

The simulation procedure for random mismatch in MOSGRAD is similar to the procedure in the systematic variation analysis. First of all, the shape of a device can be decided by the graphical interface written by Matlab. The output from the graphical interface will be sent to the netlist generator written by C language. At this step, one netlist will be finished with the finite lump-element approach using a unit cell of 4-transistors shown in Fig. 2. During the procedure of making a netlist, the random variation information can be accommodated to the netlist directly. According to our previous research [1], if we want to predict the random variation on drain current due to the random variation on V_T, the standard deviation of V_T in the finite-element approach is dependent on the voltage from the individual element to the source [10]. Thus, in order to have the right variation information of each transistor in the netlist generated by the netlist generator, we have to know the operation voltage of each element in the device region first and then go back to accommodate the random variations to the netlist. After that, the output nelist will be sent to HSpice for simulation. With the finite-element approach, more accurate, more elements. More elements

mean more random sources. More random sources mean more runs required to reach the required confidence level for the Monte Carlo simulation in Hspice. For a large amount of elements, Spice-Type simulator will have difficulties to run Monte Carlo simulation. Fortunately, according to the discussion in the paper [10], there is an alternative but faster approach available for predicting the random mismatch.

Actually, in the mismatch research for a current mirror, the most important we care about is the drain current mismatch ratio, $\sigma(\Delta I_D)/I_{D\_Nom}$ where I_{D_Nom} is the nominal drain current through each transistor in the current mirror. In the paper [10], we proved that with given V_T variation, the variation of drain current,$\sigma^2(\Delta I_D)/I_{D\_Nom}^2$, is constant within the operation range from the deep triode to the saturation region, $V_{DS} \leq V_{GS}-V_T$, and this constant is decided by $(V_{GS}-V_T)$ and V_T variation. The important observation in [10] makes the random mismatch prediction for a current mirror with rectangular devices easier and its prediction formula is represented as

$$\frac{\sigma^2(\Delta I_D)}{I_{D\_Nom}^2} = 2\sum_{i=1}^{N_i}\sum_{j=1}^{N_j}\frac{\sigma^2(C_{i,j})}{C_{i,j,N}^2}\left(\frac{\Delta L_i \Delta W_j}{LW}\right)^2 \qquad (7)$$

where $N_i=(L/\Delta L)$, $N_j=(W/\Delta W)$, and $C_{i,j}$ and $C_{i,j,Nom}$ are the conductance and nominal conductance of the ith region respectively in the active channel. It is also found that the relative variation of conductance of the (i,j)th cell element in the region is constant when N_i is going to infinity and is given by

$$\frac{\sigma^2(C_{i,j})}{C_{i,j,N}^2} = \frac{\sigma_{i,j}^2(V_T)}{(V_{GS}-V_{TN})^2} = \frac{\tilde{A}_{VT}^2}{\Delta L_i \Delta W_j (V_{GS}-V_{TN})^2} \qquad (8)$$

where $\tilde{A}_{VT}$ represents the inherent area proportionality constant what is not an extracted value, A_{VT}, and V_{TN} is the nominal value of V_T. Thus, for a current mirror with rectangular devices,

there is a closed-form expression existing for predicting the random mismatch and it is given by

$$\frac{\sigma^2(\Delta I_D)}{I_D^2} = 2\sum_{i=1}^{N_i}\sum_{j=1}^{N_j} \frac{\tilde{A}_{VT}^2 / \Delta L_i \Delta W_j}{(V_{GS}-V_{TN})^2} \left(\frac{\Delta L_i \Delta W_j}{LW}\right)^2 = \frac{2\tilde{A}_{VT}^2}{(V_{GS}-V_{TN})^2} \sum_{i=1}^{N_i}\sum_{j=1}^{N_j} \frac{\Delta L_i \Delta W_j}{(LW)^2} = \frac{2\tilde{A}_{VT}^2}{(V_{GS}-V_{TN})^2 (LW)} \quad (9)$$

The equation can also be expressed with the variation of differential V_T, $\tilde{A}_{\Delta VT}$, as

$$\frac{\sigma^2(\Delta I_D)}{I_D^2} = \frac{2\tilde{A}_{VT}^2}{(V_{GS}-V_{TN})^2 (LW)} = \frac{\tilde{A}_{\Delta VT}^2}{(V_{GS}-V_{TN})^2 (LW)} \quad (10)$$

This formula (10) is only valid with devices that have uniform current density. However, the part we are more interested in is the simulation for non-rectangular devices. Unfortunately, the current density for arbitrary-shape devices is usually not uniform and it is also very difficult to find a general closed-form formula for a non-rectangular device. Thus, the finite-element approach is a more reasonable solution to predict the matching performance of non-rectangular devices.

In Fig. 12a, current almost flows through the shadow area named as A1 and thus only the elements flowed by current have more significant contributions to current variations. The elements in the shadow area named as A2 only have very few effects to the current variations. This implies that the variation contribution on current variation from each cell element in the active channel is not uniform. However, we also found that, for a non-rectangular device, the current variation within the triode region is same as that when it is operating in the saturation region, $V_{DS}=V_{GS}-V_T$, [10]. This observation simplifies the prediction of random mismatch with non-rectangular devices because the characteristics of a device working in the deep triode region are the same as that of a resistor. Thus we can treat a non-rectangular transistor as a resistor what has the same shape as that of the non-

rectangular transistor, so next important step is to calculate how much current flows through and voltage drops across a cell element and then investigate the contribution weight to the current variation. To involve this step into MOSGRAD, a modification has to be done in the procedure of creating a netlist and the unit cell of 4 transistors will be replaced by a cell of 4 resistors shown in Fig. 12b. In the unit cell of resistor, each resistor is equal to R/2 ohms if the resistance of a unit is equal to R ohms. The output nelist from the netlist generator will then be simulated by HSpice and the current and voltage distribution across the active region will be able to be read out from the HSpice output file. This means that the voltages, V(i,j), V(i-0.5,j), V(i+0.5,j), V(i,j-0.5), and V(i,j+0.5) in Fig. 12b with each element can be read out from the HSpice output file.

The total variation on I_D can be expressed as the summarization of variation from each cell element with its contribution weight. The contribution weight can be derived from the current and voltage distribution across the region and expressed as

$$W(i,j) = \frac{dI_{D(i,j)} dV_{(i,j)}}{I_D (V_D - V_S)} \tag{11}$$

where $dI_{D(i,j)}$ and $dV_{(i,j)}$ represent the current through and the voltage across the (i,j)th cell element respectively. For each cell element, there are two possible currents, dI_i and dI_j, and voltage drops, dV_i and dV_j shown in Fig. 12b. In this approach, the maximum current flow and voltage drop will be assumed dominated and they can be represented as

$$dI_{D(i,j)} = \max(dI_i, dI_j) \tag{12}$$

$$dV_{(i,j)} = \max(dV_i, dV_j) \tag{13}$$

Because $dV_{(i,j)}$ can be read out and derived from the HSpice output file, the $dI_{D(i,j)}$ can be calculated by

$$dI_{D(i,j)} = \frac{dV_{(i,j)}}{R} \tag{14}$$

Then, the drain current variation ratio, $\sigma^2(\Delta I_D)/I_D^2$, can be expressed as

$$\frac{\sigma^2(\Delta I_D)}{I_D^2} = 2\sum_{i=1}^{N_i}\sum_{j=1}^{N_j}\frac{\sigma_{i,j}^2(R)}{R_{i,j,N}^2}(W(i,j))^2 = 2\sum_{i=1}^{N_i}\sum_{j=1}^{N_j}\frac{\sigma_{i,j}^2(V_T)}{(V_{GS}-V_{TN})^2}\left(\frac{dI_{D(i,j)}dV_{(i,j)}}{I_D(V_D-V_S)}\right)^2 \tag{15}$$

If each cell element has an equal size of length, ΔL, and width, ΔW, the equation (13) can be rewritten as

$$\frac{\sigma^2(\Delta I_D)}{I_D^2} = 2\frac{\tilde{A}_{VT}^2}{\Delta L\Delta W(V_{GS}-V_{TN})^2}\sum_{i=1}^{N_i}\sum_{j=1}^{N_j}\left(\frac{dI_{D(i,j)}dV_{(i,j)}}{I_D(V_D-V_S)}\right)^2 \tag{16}$$

To have a clear picture on the random simulation procedure in MOSGRAD, the simulation diagram flow is shown in Fig. 13.

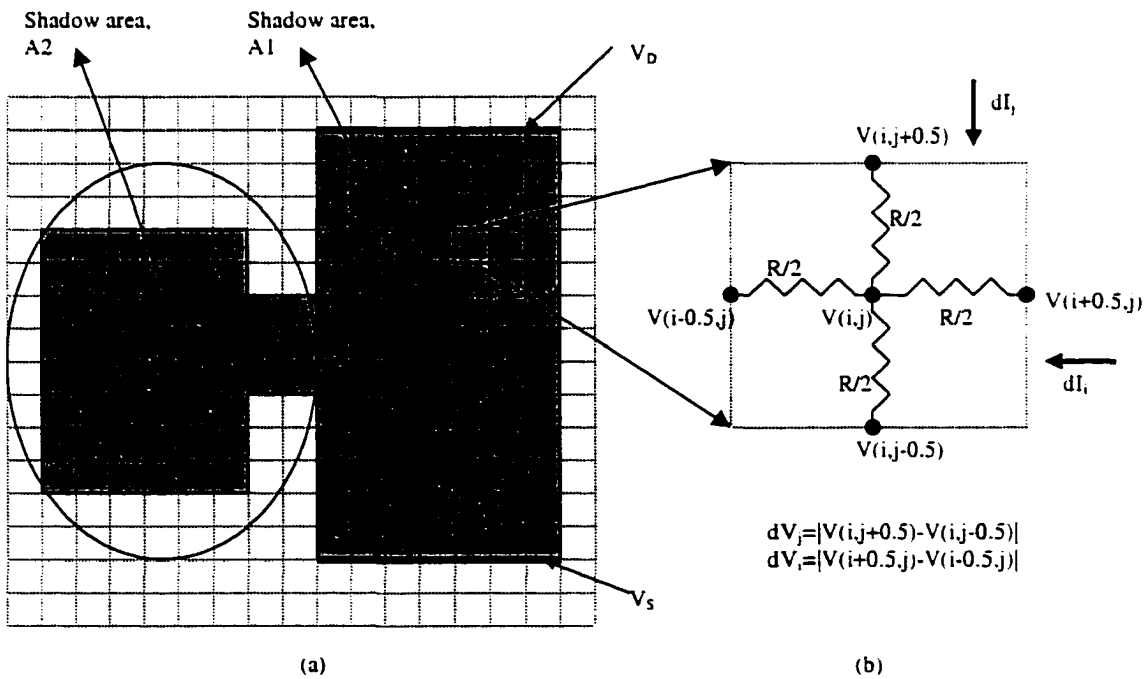


Fig. 12 Non-rectangular device and a unit cell of 4 resistor

Next, we will show several simulation results for current mirrors with rectangular and non-rectangular shapes by using this approach. One rectangular and two non-rectangular devices, named as rectangular, trapezoid and waffle respectively, are shown in Fig. 14. The simulation results with different area sizes for the device shapes shown in Fig. 14a, 14b, and 14c, are summarized into three tables, Table 1a, 1b, and 1c, respectively. In these simulations, $\tilde{A}_{VT}$ is assumed as 10mV·μm ($\tilde{A}_{\Delta VT}$ as 14.14mV·μm), V_G as 2.8V, V_D as 1.7V, V_S as 0V, and V_{TN} as 0.8V. The random mismatch results for the layout shapes in Fig. 14 are plotted as a function of $1/\sqrt{Area}$ in Fig. 15. From the Fig. 15, the rectangular devices basically follow the law of area, but the trapezoid and waffle devices do not follow the law of area because of the non-uniform current density. The A_{VTO} and $A_{\Delta VTO}$ are usually extracted from the current measurements directly and thus the results in Fig. 16 imply that the extracted A_{VTO} and $A_{\Delta VTO}$ are shape dependent.

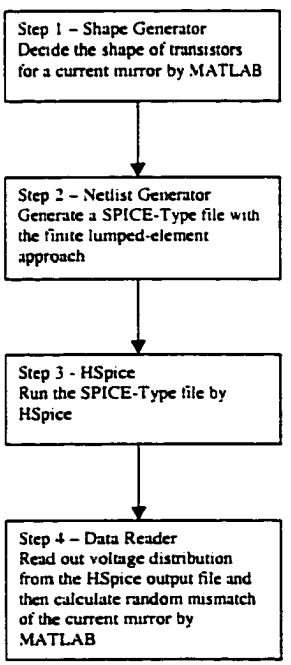


Fig. 13 Simulation diagram flow for random mismatch

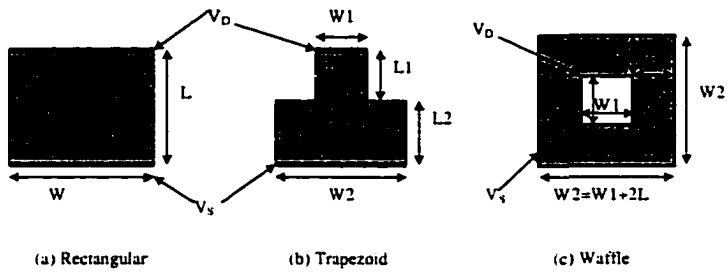


Fig. 14 Device shapes of current mirrors

Table 1a. Simulation Summary of Rectangular Device shown in Fig. 14a

	W (μm)	L (μm)	Area of Current Mirror (μm^2)	Random Mismatch $\sigma(\Delta I_D)/I_{D\_Nom}$ (%)
1	20	20	400	4.1595e-2
2	20	30	600	3.3962e-2
3	40	20	800	2.9412e-2
4	40	40	1600	2.0797e-2

Table 1b. Simulation Summary of Trapezoid Device shown in Fig. 14b

	W1 (μm)	W2 (μm)	L1 (μm)	L2 (μm)	Area of Current Mirror (μm^2)	Random Mismatch $\sigma(\Delta I_D)/I_{D\_Nom}$ (%)
1	10	30	10	10	400	5.7841e-2
2	10	30	10	20	700	4.8211e-2
3	10	40	20	20	1000	4.3557e-2
4	20	60	20	20	1600	2.9093e-2

Table 1c. Simulation Summary of Waffle Device shown in Fig. 14c

	W1 (μm)	L (μm)	Area of Current Mirror (μm^2)	Random Mismatch $\sigma(\Delta I_D)/I_{D\_Nom}$ (%)
1	5	8	416	5.0445e-2
2	5	10	600	4.4909e-2
3	10	10	800	3.3480e-2
4	15	16	1664	2.5659e-2

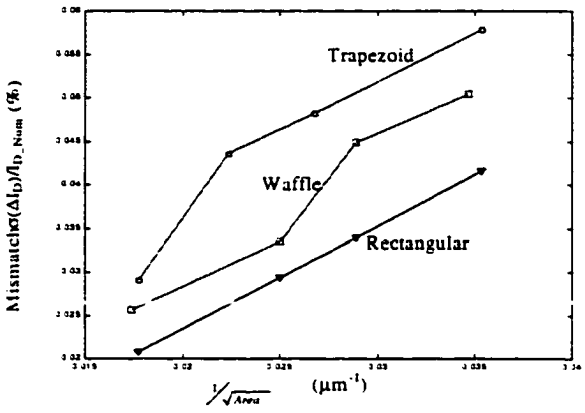


Fig. 15 Simulation results with different shapes and area sizes of current mirrors

IX. Conclusion

A CAD tool, MOSGRAD, suitable for predicting the systematic mismatch in the presence of arbitrary parameter gradients and random mismatch at current mirrors for arbitrary shapes has been introduced. Comparison of experimental and simulation results showed good correlation. It has also uncovered some fundamental limitations in the previously unquestioned relationship between the effects of random variations on circuit performance and gate area.

Acknowledgements

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CHAPTER 4. CURRENT MIRROR LAYOUT STRATEGIES FOR ENHANCING MATCHING PERFORMANCE

A paper accepted by the Journal of Analog Integrated Circuits and Signal Processing

Mao-Feng Lan, Anilkumar Tammineedi, and Randall L. Geiger

Abstract

This paper proposes new current mirror layout strategies to reduce the matching sensitivity to the linear parameter gradients. Effects of threshold gradients across a mirror on the matching characteristics of current mirrors are discussed. The performance of new and existing layouts are compared for threshold voltage gradients at arbitrary angles through the active area. Simulation results show a significant improvement in matching characteristics of the proposed structures over what is achievable with existing layout techniques in demanding applications.

I. Introduction

Paralleling the increasing demand for cost-effective integrated high-end linear and mixed-signal systems is the need for improved matching performance in basic circuit blocks because the system performance is dominated by the matching characteristics of basic circuit blocks such as current mirrors and differential amplifiers. Researchers have proposed models for predicting the matching characteristics of closely-placed devices [1-3], but these models have been used almost exclusively to assess performance characteristics of circuits and layout techniques that have been well-known for over two decades. Further, these models

have fundamental limitations in characterizing the effects of systematic parameter variations through the channel region of transistors.

It is generally agreed that the matching characteristics of closely placed devices can be attributed to systematic and random variations in both geometric parameters and process parameters. The traditional approach for managing the effects of random variations is to increase the area of the matching-critical devices to the level that the random mismatch effects are reduced to an acceptable level. It is often more difficult to compensate for the systematic variations which may be random at the wafer or even die level but which are highly correlated at the basic circuit block level. Because the area and pitch of a current mirror is relatively small to that of a die, systematic variations are generally assumed to be represented by linear gradients in the matching-sensitive part of the circuit and common centroid layout techniques such as that of Fig. 1 are widely used to minimize the effects of the linear gradients. The most standard common centroid layout technique for a current mirror or a differential pair uses two cross-connected pairs of rectangular transistors. Felt et. al. [3] have reported that the effects of systematic variations are often comparable to the effects of random variations even with good layout techniques thus affirming the need for managing simultaneously the effects of both systematic and random variations. Some of the systematic variations are often mistakenly assumed to be random (an assumption that can cause significant errors in a statistical analysis because of the inherent correlation of these parameters). We believe that the impact of not correctly handling the systematic variations is even more significant than suggested by Felt et. al, in the design of high-end linear circuits.

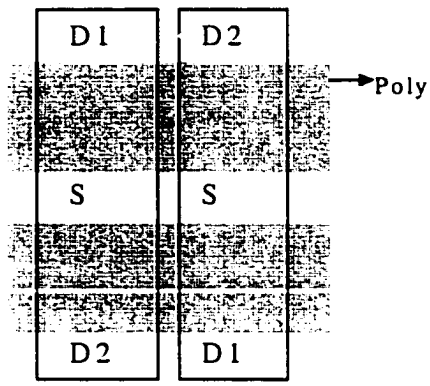


Fig.1. Common Centroid Layout

Although variations in threshold voltage (V_T), mobility (u), C_{OX}, along with some other parameters affect mirror matching, the dominant effects are generally threshold voltage variations. In this paper, only the effects of spatially dependent threshold voltage variations are considered for various layouts to compare matching characteristics, but the reduced sensitivity to gradients in other parameters parallel that observed for V_T gradients in the proposed structures.

A basic current mirror is depicted in Fig. 2. The input port is at the drain of transistor M1, the output is at the drain of transistor M2 and the sources are common. Five different common layouts for this current mirror are shown in Fig. 3. Fig. 3(a) shows the simple layout technique. Although parameter gradients that occur in the direction from drain to source (designated as "vertical" in Fig. 3) cause no device matching problems with this structure, the matching performance degrades substantially if there are substantial "horizontal" components of the gradient. The interdigitized layout structures of Fig. 3(b) and Fig. 3(c) have a reduced sensitivity to horizontal components of the gradient. The two-segment

interdigitized structure of Fig. 3(b) is a common centroid layout and, as such, most existing models predict linear parameter gradients will not cause any mismatch if this is used to form a current mirror or cause any offset voltage if it is used as the source-coupled pair in a differential amplifier. In what follows, it will be shown that the gradient effects are still substantial on the interdigitized layout of Fig. 3(b) and 3(c). The two-segment common centroid layouts of Fig. 3(d) and Fig. 3(e) generally offer better matching performance than the other structures presented in the figure. The common centroid layout technique is currently being widely used and it does reduce systematic gradients when compared to the simple and interdigitized techniques. Since these structures both have a common centroid, most existing models predict complete immunity to linear gradient effects. In what follows, it will be shown that even the structures of Fig. 3(d) and 3(e) have a systematic mismatch component that can be significant in applications with stringent matching requirements.

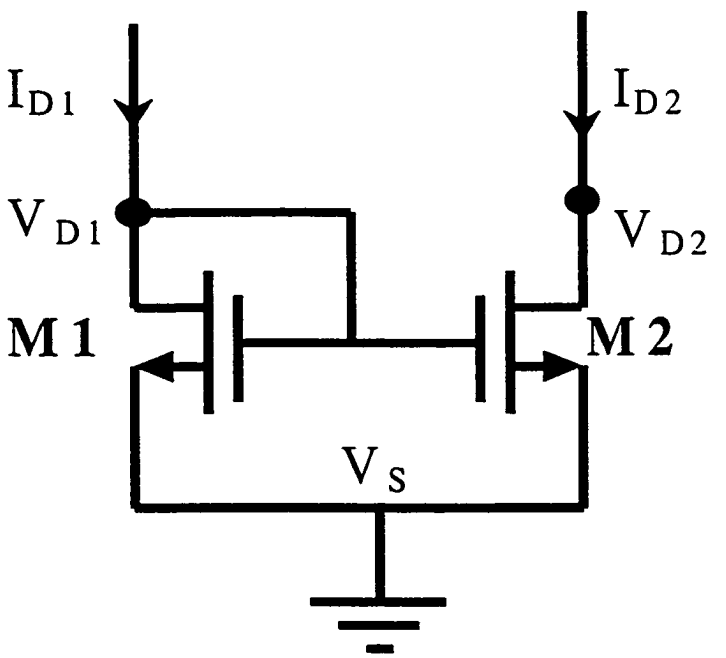
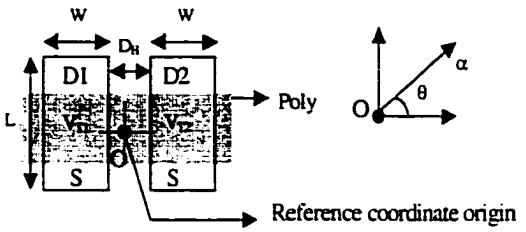
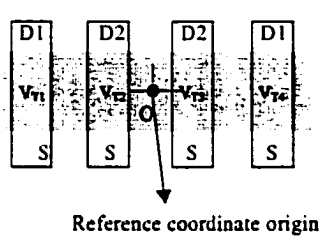


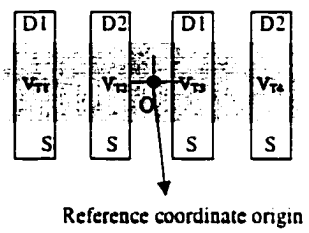
Fig. 2. Basic Current Mirror Circuit



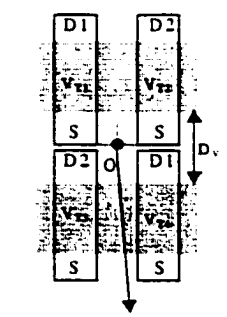
(a) Simple Layout



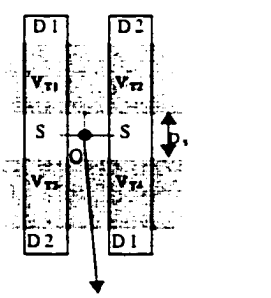
(b) Interdigitized Type I



(c) Interdigitized Type II



(d) Common Centroid Type I



(e) Common Centroid Type II

Fig. 3. Existing Current Mirror Layout Techniques (D1 is Drain of M1, D2 is Drain of M2, S is Common Source, and O : Reference Point)

In this paper, several new common-centroid layout techniques are introduced. One uses an interconnection of two 4-segment rectangular transistors. The balance are non-rectangular structures in which the active region is continuously distributed between the input and output ports of the current mirror and in which there is no obvious equivalent lumped two-transistor equivalent circuit. In contrast to existing mirror circuits in which the matching-sensitive part of the circuit is comprised of two source-coupled transistors, the nonrectangular structures discussed in this paper are 4-terminal devices that can be viewed as dual-drain transistors. It will be shown that the proposed layout structures can be designed so that the mirror gain is less sensitive to the linear parameter gradients than what is achievable with the widely used two-segment common centroid structures.

II. Gradient Modeling

In this section, the effects of threshold voltage gradients on the matching performance of current mirrors are investigated. In particular, the effects of threshold voltage gradients at any angle across a wafer for interdigitized and common-centroid layouts are compared with the matching characteristics of a simple mirror layout. The parameter gradients are commonly modeled in a distributed way through the active devices themselves, and thus threshold voltage is modeled as a distributed position-dependent parameter through the active devices, $V_T(x,y)$. The widely used approach for predicting the effects of the threshold gradient is based upon deriving an equivalent threshold voltage [1] for the device as given by the following equation.

$$V_{Teq} = \frac{\iint_{Active\ Area} V_T(x,y)\,dx\,dy}{Active\quad Area} \tag{1}$$

and using this threshold voltage in the existing lumped-parameter models of a transistor.

If the threshold gradient amplitude is α and the gradient direction is θ as indicated in Fig. 3, it follows that for the simple current mirror structure (Fig. 3(a)):

$$V_{T1} = V_{TN} - \alpha(\frac{W}{2} + \frac{D_H}{2})\cos\theta \qquad (2)$$

$$V_{T2} = V_{TN} + \alpha(\frac{W}{2} + \frac{D_H}{2})\cos\theta \qquad (3)$$

where

1) D_H is the minimum separation, usually 4 lambda, between the two drain diffusions, D1 and D2.
2) V_{T1} and V_{T2} are the threshold voltages of the two transistors of equal sizes W/L
3) V_{TN} is the threshold voltage at the coordinate reference point O in Fig. 3(a).

If the equivalent V_T equation (1) is applied to the Type I interdigitized layout of Fig. 3(b), transistors M1 and M2 have the same threshold voltage given by the following equation.

$$V_{TD1} = V_{TD2} = V_{TN} \qquad (4)$$

This equivalent threshold voltage was expected since this is a common centroid layout. This model predicts perfect matching can be achieved using this layout structure. However, experimental results have not been in accordance with the perfect matching prediction thus leading to the conclusion that this simple integral model can significantly skew matching results. An alternative approach to modeling the mismatch effects using a segmented integral model does give better results. In this approach, instead of treating transistor M1 as a single transistor and using equation (1) to predict the equivalent threshold voltage, we will assume

M1 is modeled as the parallel connection of two lumped transistors in which the integral model of (1) is used to independently obtain the equivalent threshold voltage of each of the two components. For a multi-segment layout, the equivalent threshold voltage for each segment is predicted using the integral model of (1), and these transistors are then placed in parallel to form a circuit that represents the transistor designed as M1 or M2 in Fig. 2. We refer to this modeling approach as the segmented integral model. In general, using this approach, there does not exist an equivalent threshold voltage for the transistor M1, and the I-V characteristics of the parallel-connected segments are not identical to the I-V characteristics of an equivalent single transistor if the same functional form for the lumped model is used for modeling all segments. Formally, the threshold voltage for the Kth segment in the segmented integral model is given by

$$V_{T_{eq},K} = \frac{\iint_{Active\ Area\ .\ K} V_T(x,y)\,dx\,dy}{Active\quad Area\ .\ K} \tag{5}$$

Using this approach, the threshold voltages for the simple structure remain the same as before while those of the four unit transistors for the Type I interdigitized structure are given by,

$$V_{T1} = V_{TN} - \alpha\left(\frac{3W}{4} + \frac{3D_H}{2}\right)\cos\theta \tag{6}$$

$$V_{T2} = V_{TN} - \alpha\left(\frac{W}{4} + \frac{D_H}{2}\right)\cos\theta \tag{7}$$

$$V_{T3} = V_{TN} + \alpha\left(\frac{W}{4} + \frac{D_H}{2}\right)\cos\theta \tag{8}$$

$$V_{T4} = V_{TN} + \alpha\left(\frac{3W}{4} + \frac{3D_H}{2}\right)\cos\theta \tag{9}$$

where V_{T1} and V_{T4} correspond to the two segment transistors of M1 and V_{T2} and V_{T3} correspond to the two segment transistors of M2. The four expressions also hold for the Type II interdigitized layout of Fig. 3(c) where V_{T1} and V_{T3} correspond to the two segment transistors of M1 and V_{T2} and V_{T4} correspond to the two segment transistors of M2. Similarly, threshold voltages for the four segment transistors were determined for the common centroid Type I and Type II layouts of Fig. 3(d) and 3(e) and are given by,

$$V_{T1} = V_{TN} - \alpha(\frac{W}{4} + \frac{D_H}{2})\cos\theta + \alpha(\frac{D_{V/S}}{2} + \frac{L}{2})\sin\theta \quad (10)$$

$$V_{T2} = V_{TN} + \alpha(\frac{W}{4} + \frac{D_H}{2})\cos\theta + \alpha(\frac{D_{V/S}}{2} + \frac{L}{2})\sin\theta \quad (11)$$

$$V_{T3} = V_{TN} - \alpha(\frac{W}{4} + \frac{D_H}{2})\cos\theta - \alpha(\frac{D_{V/S}}{2} + \frac{L}{2})\sin\theta \quad (12)$$

$$V_{T4} = V_{TN} + \alpha(\frac{W}{4} + \frac{D_H}{2})\cos\theta - \alpha(\frac{D_{V/S}}{2} + \frac{L}{2})\sin\theta \quad (13)$$

where D_V and D_S are the minimum required distances between the two channels as shown in Fig. 3(d) and Fig. 3(e), respectively. V_{T1} and V_{T4} correspond to the two segment transistors of M1 and V_{T2} and V_{T3} correspond to the two segment transistors of M2. It is apparent from these equations that the threshold voltages of the individual segments differ and are dependent upon the magnitude and angle of the gradient as well as the geometries of the segments. What is less apparent is how these threshold variations affect matching performance.

The above equations were used to simulate mismatch for the five mirror layouts and for a gradient of fixed amplitude but arbitrary direction. In these simulations, it was assumed that V_{TN}=0.7339V, α=1mV/um, W=40um, L=40um, and D_H=4um. The gradient direction was varied between 0° and 360°. For a fair comparison, mismatch for all the structures were

measured with the same active area and the same equivalent W/L. Here, mismatch is defined by,

$$Mismatch = \frac{I_{D2} - I_{D1}}{I_{D1}} x100\ \% \qquad (14)$$

where I_{D1} and I_{D2} are the input and output currents as depicted in Fig. 2. The simulation results for an input current of I_{D1}=77.5μA are shown in Fig 4. In these simulations, the voltages V_{DS2} was set equal to the resultant V_{DS2} to remove mismatch due to the output impedance.

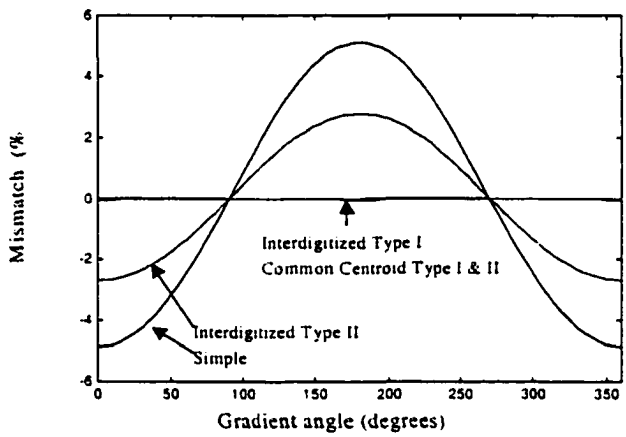


Fig. 4. Comparison of Systematic Mismatch for Simple, Interdigitized and Common Centroid Layouts

From these simulation results, it can be seen that interdigitized Type I, common centroid Type I and common-centroid Type II have very good matching characteristics relative to the other two structures. An expanded view of the latter three results is shown Fig. 5. From these simulation results, it can be observed that the interdigitized Type I layout has mismatch characteristics with minimum deviations at θ = 90° and 270° and maximum

deviations of about –0.04% at 0° and 180°. Further, the mismatch is always negative. The common centroid Type I and II layouts have better and similar matching performance with maximum mismatch magnitudes of about 0.02% occurring at θ = 45°, 135°, 225° and 315° for the 1 mV/μm gradient.

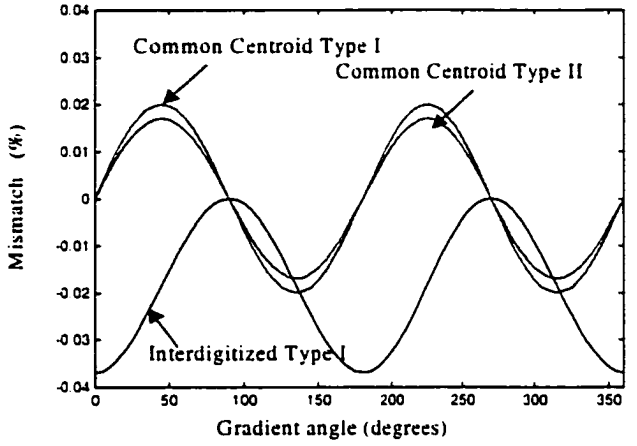


Fig. 5. Comparison of Interdigitized and Common Centroid Layouts in closer detail

The simulation results show that the matching characteristics are strongly a function of the angle of the threshold voltage gradient across a die and that, for any angle, the effects of the threshold gradient for the common centroid layouts is small. The results also show, in contrast to the well-accepted premise that the effects of linear gradients can be readily modeled [4] and are inherently canceled in common centroid structures [3], that the threshold gradients through the devices themselves create an angle-dependent gradient even in common centroid structures. The issue of the validity of using the segmented integral model does deserve attention since it was shown that the integral model itself introduces substantial errors in matching-critical applications. The results that were presented in this section that are based upon simple closed-form expression for lumped model parameter such as (6)-(9) or

(10)-(13) are in close agreement to what is attainable with a full two-dimensional simulation [5] of the distributed device parameters for the common centroid and interdigitized structures of Fig. 3. Simulation results for these structures based upon a two-dimensional simulation are discussed later in this paper.

III. Proposed Layout Technique

A. Four-Segment Layout Structure

A new four-segment common centroid structure that offers improvement in matching over what is achievable with the two-segment common centroid techniques is shown in Fig. 6. The proposed layout technique has the property that it also minimizes the mismatch at 45°, 135°, 225° and 315° angles where the two-segment common centroid structures exhibit maximum mismatch. It can be observed that in the common centroid layout technique of Fig. 3(d) and Fig. 3(e), the layout is the same when rotated by 180°, thus canceling the mismatch at 90° while having a maximum at 45°. In the proposed technique, the layout is the same when rotated by 90°, thus canceling the mismatch at 45°. In the proposed structure, each transistor is segmented into 4 unit transistors since the source and the gate are common for the current mirror, the source and gate are shared for all the eight unit transistors.

The segmented integral model was used to evaluate the matching characteristics of the proposed technique paralleling the analysis for the layout techniques of Fig. 3 discussed in the previous section. The threshold voltages of eight unit transistors in Fig. 6 are given by:

$$V_{T1} = V_{TN} - \alpha\left(\frac{D_H}{2} + \frac{W}{8}\right)\cos\theta + \alpha\left(\frac{3D_H}{2} + \frac{W}{4} + \frac{L}{2}\right)\sin\theta \tag{15}$$

$$V_{T2} = V_{TN} + \alpha\left(\frac{D_H}{2} + \frac{W}{8}\right)\cos\theta + \alpha\left(\frac{3D_H}{2} + \frac{W}{4} + \frac{L}{2}\right)\sin\theta \tag{16}$$

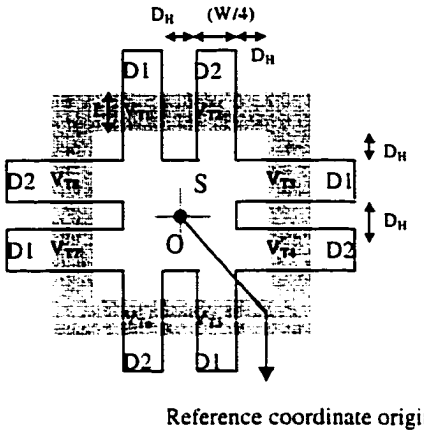


Fig. 6. Proposed Current Mirror Layout Technique – Four-Segment Structure

$$V_{T3} = V_{TN} + \alpha\left(\frac{3D_H}{2} + \frac{W}{4} + \frac{L}{2}\right)\cos\theta + \alpha\left(\frac{D_H}{2} + \frac{W}{8}\right)\sin\theta \tag{17}$$

$$V_{T4} = V_{TN} + \alpha\left(\frac{3D_H}{2} + \frac{W}{4} + \frac{L}{2}\right)\cos\theta - \alpha\left(\frac{D_H}{2} + \frac{W}{8}\right)\sin\theta \tag{18}$$

$$V_{T5} = V_{TN} + \alpha\left(\frac{D_H}{2} + \frac{W}{8}\right)\cos\theta - \alpha\left(\frac{3D_H}{2} + \frac{W}{4} + \frac{L}{2}\right)\sin\theta \tag{19}$$

$$V_{T6} = V_{TN} - \alpha\left(\frac{D_H}{2} + \frac{W}{8}\right)\cos\theta - \alpha\left(\frac{3D_H}{2} + \frac{W}{4} + \frac{L}{2}\right)\sin\theta \tag{20}$$

$$V_{T7} = V_{TN} - \alpha\left(\frac{3D_H}{2} + \frac{W}{4} + \frac{L}{2}\right)\cos\theta - \alpha\left(\frac{D_H}{2} + \frac{W}{8}\right)\sin\theta \tag{21}$$

$$V_{T8} = V_{TN} - \alpha\left(\frac{3D_H}{2} + \frac{W}{4} + \frac{L}{2}\right)\cos\theta + \alpha\left(\frac{D_H}{2} + \frac{W}{8}\right)\sin\theta \tag{22}$$

With this model, it can be readily shown that the mismatch for the proposed technique is zero at 45°, 90°, 135°, 180° and so on, giving a big improvement in matching characteristics over that of the two-segment common centroid layout of Fig. 3. A disadvantage of the proposed technique is the requirement of more silicon-area. When the silicon area increases, the assumption that the gradient remains linear throughout the entire matching-critical region

may not be completely justifiable. Nonlinear gradients are, in general, not inherently cancelled with common centroid layouts. Some new layout structures that require less area than what is required for the four-segment layout of Fig. 6 are discussed in the following section.

For the same reason the integral model gives incorrect results with segmented transistors; even the errors caused by the segmented integral model become significant when close matching is expected. A two-dimensional simulator [5] was developed for predicting matching characteristics in the presence of either linear or non-linear gradients through the active area of the devices. The simulator can be used to predict the matching characteristics of an arbitrary layout of any size for arbitrary gradients in threshold voltage or any other process parameters.

The four-segment structure (Fig. 6), the interdigitized Type I layout, the common centroid Type I layout and the common centroid Type II layout were simulated with this two-dimensional simulator for the 2μm CMOS process available through MOSIS. The mismatch characteristics as a function of angle are shown in Fig. 7. In this simulation, the same device size and gradient parameters used in Section II were used. It can be seen that the four-segment layout improves the matching performance by at least two orders of magnitude over what is achievable with the two-segment common centroid layouts in the presence of linear threshold gradients. The simulation results for the proposed four-segment layout structure in Fig. 7 are expanded in Fig. 8. It is observed that the mismatch of the proposed four-segment structure is zero at angles of 0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°. Table 1 summarizes the worst case mismatch in the structures simulated. Also shown in this table is a comparison of the results as predicted by the simple integral model, the segmented integral

model and the actual distributed parameter model. The maximum effective achievable resolution is calculated from the results of the simulator such that the worst case mismatch is less than ½ LSB relative to full-scale. It can be seen that in the presence of perfectly linear gradients at 1 mV/μm, the two-segment common centroid structure can achieve only about 12-bit resolution while the proposed structure can achieve 18-bit resolution showing a big improvement in matching with the new layout. It should be emphasized that the results are valid only for a perfectly linear gradient of 1mV/μm and the resolution would be lower if the gradient is non-linear or if other non-idealities such as random variations in either dimensional or process parameters were included.

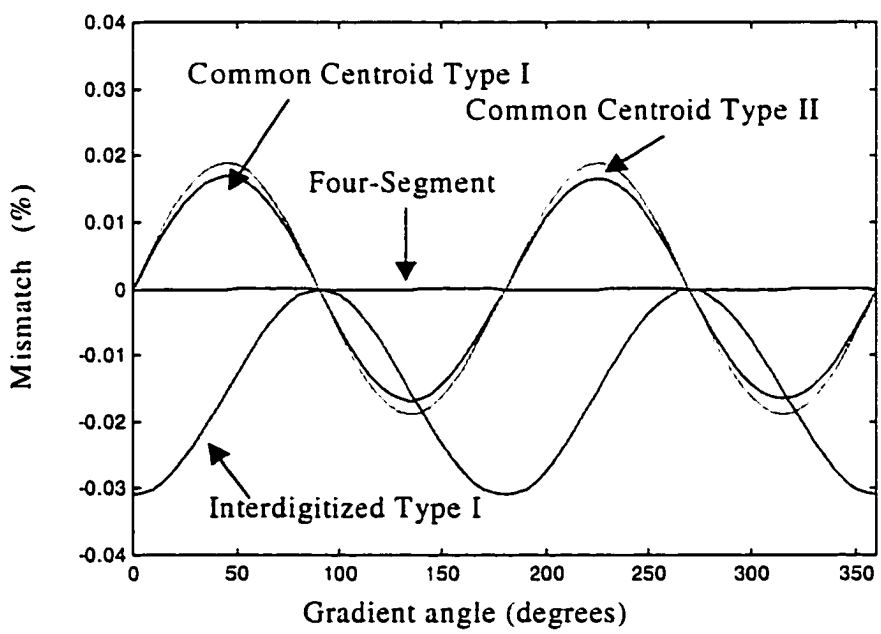


Fig. 7. Comparison of Interdigitized, two-Segment Common Centroid and Four-Segment Layouts

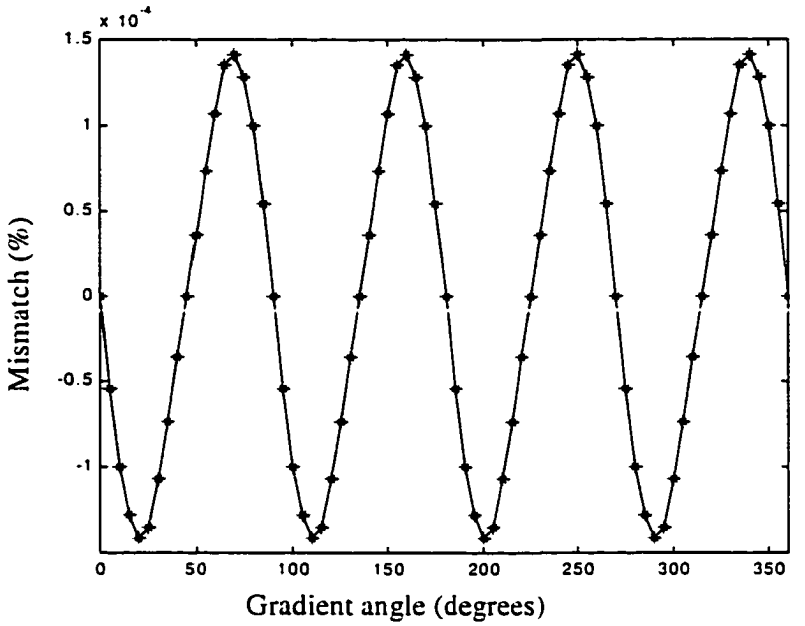


Fig. 8. Simulation result of Proposed Four-Segment Common Centroid Layout

Table 1. Comparison of various structures with a linear gradient of 1mV/um

Structure	Worst Mismatch (%)			
	Simple integral model	Segmented integral model	Distributed simulator	Effective Resolution
Simple	5.1092	5.1092	4.8807	3-bit
Interdigitized Type I	0	3.6918e-2	3.0885-2	11-bit
Interdigitized Type II	2.7552	2.7547	2.6329	4-bit
Two-Segment Common centroid Type I	0	2.0005e-2	1.6966e-2	12-bit
Two-Segment Common centroid Type II	0	1.6928e-2	1.8949e-2	12-bit
Four-Segment Common Centroid Structure	0	2.0966e-14	1.4090e-4	18-bit

B. Non-Rectangular Structure

A non-rectangular layout of a current mirror is shown in Fig. 9. In this circuit, the polysilicon region (gray) and the two regions labeled D1 are connected together and serve as the input current node. The diffusion labeled S is thought of as the 'source' for the device and is connected to ground. The two regions labeled D2 are connected together and serve as the output current node. This is a special case of what is occasionally termed a "waffle transistor" and will be designated as a "waffle structure" throughout the remainder of this paper. To avoid possible confusion, the distinction between the waffle structure of Fig. 9 and the conventional waffle transistor will be clarified. In a waffle transistor, the diffusion "islands" internal to the gate polysilicon are alternately source and drain connections. In the waffle layout of the current mirror of Fig. 9, there is no inherent two-transistor equivalent circuit but instead it is a distributed two-segment dual-drain device in which the source comprises the perimeter of the polysilicon region and the dual drains are alternately connected islands internal to the gate polysilicon.

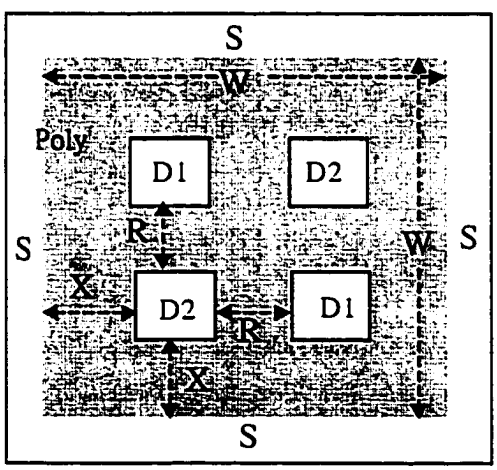


Fig. 9. Non-Rectangular Current Mirror Layout Technique (Waffle Structure)

The active region is shared between the two drains in this layout. In what follows, it will not only be shown that this two-segment dual-drain device performs as a current mirror but that in the presence of parameter gradients, if properly designed, it can offer better matching performance than what is achievable with the standard two-segment common centroid layouts of Fig. 3(d) and Fig. 3(e). Without going into a rigorous definition of what constitutes a "common centroid" characteristic in a distributed dual-drain transistor, it is sufficient to say that it can be shown that the waffle structure is also a common centroid layout.

Because the waffle mirror is not representable with two distinct source-connected transistors, standard modeling techniques cannot be applied to the structure. Because the simulator [5] is able to predict the matching characteristics of an arbitrary layout of any size for arbitrary gradients, it will be used to predict the matching characteristics of the waffle mirror structure in the presence of linear threshold gradient.

For the waffle structure of Fig. 9, the drain current and matching performance are affected by both the size and the positions of the drain diffusions in the layout. The relationship between the drain current (with gate tied to D1 and D2 left open) and the positions of the drain diffusions for the 2μm CMOS process available through MOSIS was evaluated using the simulator. Results are given in Fig. 10. In this figure, the y axis is the magnitude of drain current and the x axis is given by the ratio of X divided by W, where X (shown in Fig. 9) is the space from a diffusion to the source edge and W is the width of the device that is assured to be square. In this simulation, the total active area was kept fixed at (80μmx80μm-4x8μmx8μm)=6144 μm^2 as was the size of the drain diffusions which were

8μm x 8μm. It is observed that the drain current increases when the drain contacts approach to the edge of the source.

As described in the previous section, the waffle layout structure is the same when rotated by 180°, thus canceling the mismatch at 90° while having a maximum mismatch at 45°, 135°, 225° and 315° as was the case for the two-segment common centroid structures of Fig. 3(d) and Fig. 3(e).

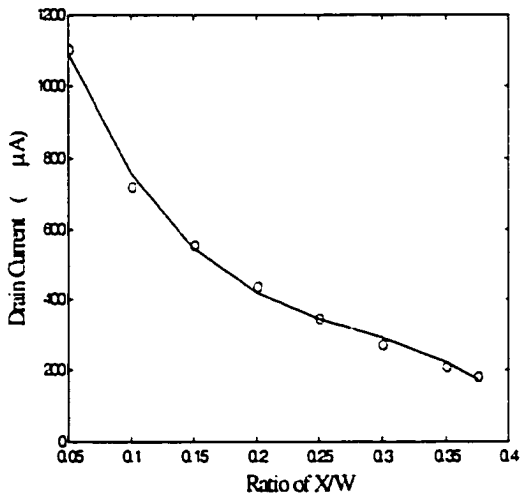


Fig. 10. Drain Currents with the Positions of Drain Contacts

The worst-direction matching characteristics of the waffle structure for a gradient of α=1mV/μm when used as a current mirror were simulated and are shown in Fig. 11 as a function of the total active area. In this simulation, the distance X was kept at (3/16)W, R was (3/8)W and the drain diffusions were square with a side length of (1/8)W. It is well known that in current mirrors implemented with rectangular transistors, the standard deviation of the random mismatch decreases with the square root of the total active area. The effects of random mismatch for the waffle structure were simulated with a value of A_{VTO} of

5.3mV. μm. The standard deviation of the mismatch expressed in percent is also shown in Fig. 11.

The results show that the random mismatch is linearly proportional to $(1/\sqrt{Active\_Area})$ and the systematic mismatch is approximately inversely proportional to $(1/\sqrt{Active\_Area})$. Thus, tradeoffs must be made between increasing the active area to reduce random mismatch effects and decreasing the area to minimize worst-case gradient effects. These same tradeoffs must be made when using conventional layout structures [1].

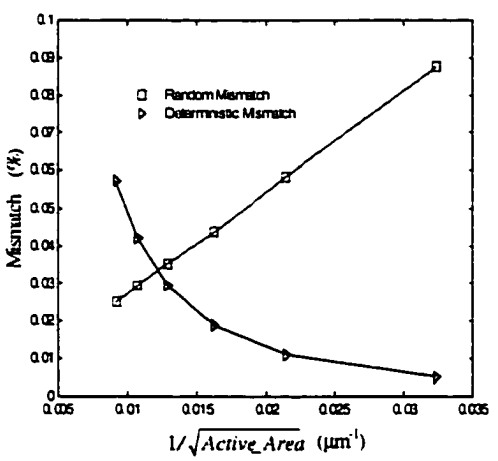


Fig. 11. Deterministic and Random Mismatches of Waffle Structure

To evaluate the matching performance, the matching characteristics of the waffle structure will now be compared with those of the two-segment common centroid structure of Fig. 3(e). In order to make a fair comparison on the matching performance, the two-segment common centroid structures are designed to have the same active areas, the same nominal drain current and the same excess bias (V_{GS}-V_T) as the waffle structures. The comparison is made for a waffle structure that is 80μm x 80μm as a function of the parameter X in Fig. 12.

The drain diffusions were fixed at 8μm x 8μm. Since changing the parameter X will result in a change in either current or excess bias voltage, we kept the excess bias fixed and allowed the current to vary while keeping the current the same in both the waffle structure and the corresponding common centroid structure of Fig. 3(e). The comparison of the worst-direction matching performance is shown in Fig. 12 for a gradient magnitude of α=1mV/μm. This figure shows that the two-segment waffle structure can offer significantly better matching performance than the two-segment common centroid structure in the presence of linear parameter gradients but also that the positioning of the drain diffusions is important. It is also observed that the matching performance of the waffle mirror structure for a fixed active area improves when the drain contacts are moved farther from the source contact.

Fig. 13 shows the mismatch as a function of angle for a waffle structure with W=80μm, X=20μm and with 8μm drain diffusions as compared with that of the two-segment common centroid structure of Fig. 3(e). As before, the same active area, current and excess bias were used for both layouts.

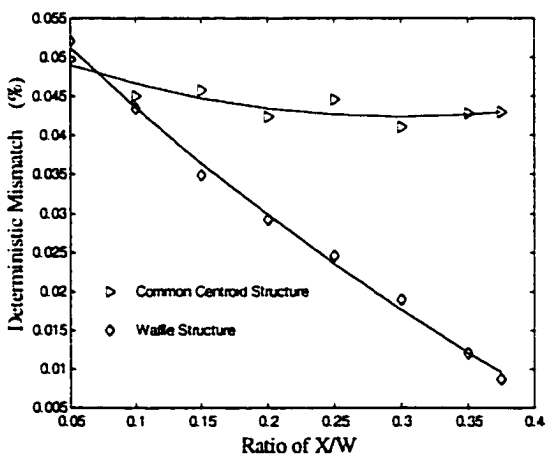


Fig. 12. Comparison of Waffle and Common Centroid Structure with a Fixed Active Area

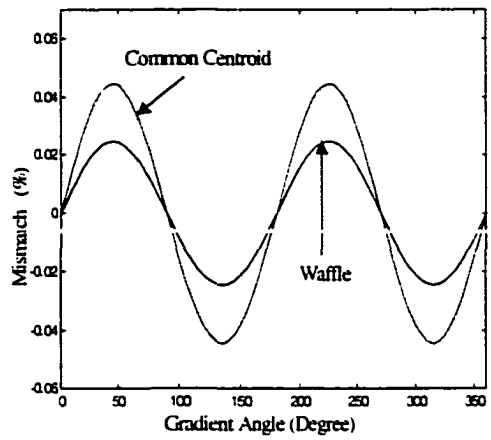


Fig. 13. Performance Comparison of Common Centroid and Waffle Structure

From a practical viewpoint, it must be emphasized that the comparative results presented in Fig. 12 are obtained for a specific parameter gradient and a specific total active area. The relative performance of the two structures is strongly dependent upon both active area and the relative positioning of the drain diffusions in the waffle structure. Different parameter gradients and/or different relationships between the excess bias and the nominal drain current will affect where the crossover in Fig. 12 in performance between the common centroid layout of Fig. 3(e) and the waffle structure occurs.

The issue of optimality of the proposed waffle structure has not yet been determined. As is apparent from Fig. 10, even for a given active area, tradeoffs between the size and location of the drain diffusions can be made. Optimal structures should offer even better performance than what was presented here.

IV. Layouts based on the Proposed Technique

As mentioned previously, the proposed four-segment layout of Fig. 6 is not particularly area efficient because it requires considerable area around the individual/common source regions. The two-segment waffle layout technique is quite compact but does not have as good matching properties as the four-segment structure of Fig. 6. Thus, the question naturally arises if it is possible to combine the advantages of these two layout techniques to generate new layouts that have improved matching and yet are area efficient. The answer is yes. Three layouts combining the advantages of two techniques are shown in Fig. 14. Although each layout configuration in Fig. 14 has different area requirements, these three layouts all not only have better area budget than the four-segment layout but also have similar matching characteristics. These layouts are common-centroid four-segment distributed channel structures. For all these structures, mismatches are minimized for linear gradients at 45°, 135°, 225° and 315°. It is beyond the scope of this paper to fairly compare the three layouts in Fig. 14 since the structures do not have the same active area, the same drain currents and the same excess bias. A general idea about how these three layouts perform, however, can be developed from the following simulations. Simulation results for the three layouts of Fig. 14 for special device dimensions and a threshold gradient of α=1mV/μm appear in Fig. 15. For the simulation of the layout of Fig. 14(a) shown in Fig. 15(a) it was assumed that X=20μm. In the simulation of the layout of Fig. 14(b) shown in Fig. 15(b), the dimensions of X=20μm and Y=4μm were used. The simulation results for the circuit of Fig. 14(c) shown in Fig. 15(c) were based upon a device dimension of X=8μm. In all cases, the voltage of the output node, drain D2, was set equal to

that at the input node, drain D1. The input currents are 117μA, 195μA, and 744μA for the layouts in Fig. 14(a), Fig. 14(b), and Fig. 14(c) respectively. It is apparent that these three layouts have at least two orders of magnitude better matching performance in the presence of linear threshold gradients than the two-segment common centroid layouts of Fig. 3(d) and 3(e) even without optimization.

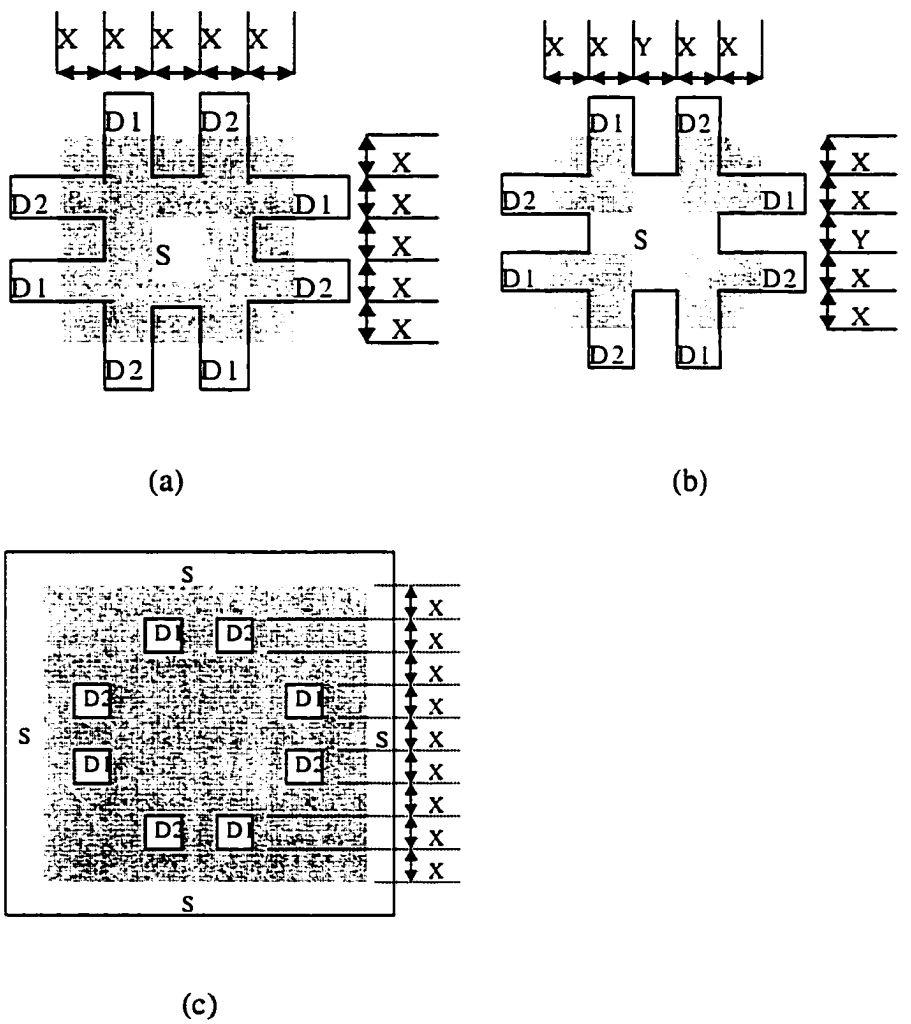
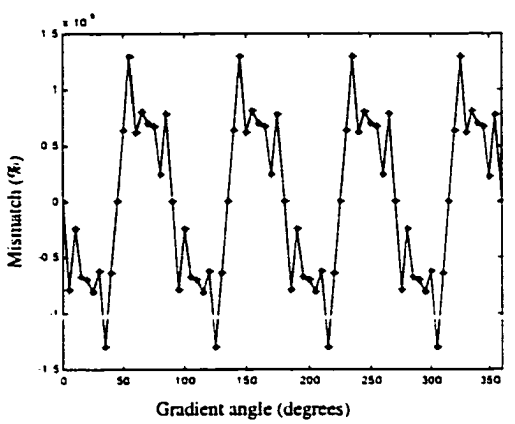
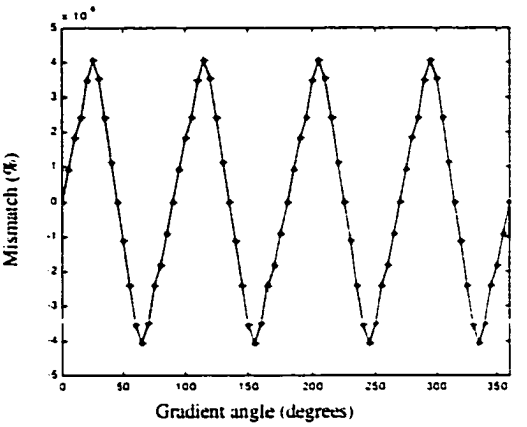


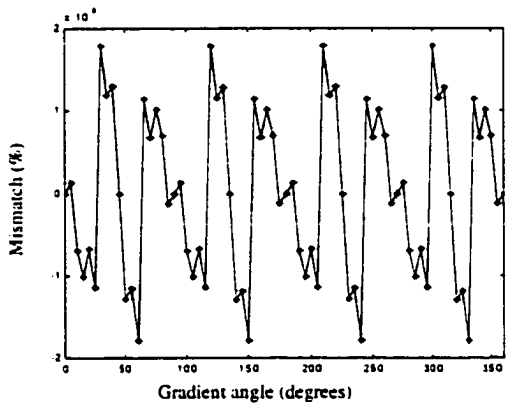
Fig. 14. Proposed Current Mirror Layout Techniques



(a)



(b)



(c)

Fig. 15. Simulation Results for Mirror Layouts of Fig 14

V. Conclusion

Several new current mirror layout techniques have been introduced that offer substantial improvements in matching characteristics over what is achievable with the simple, interdigitized and the two-segment common centroid structures in the presence of linear parameter gradients. The layout techniques include a four-segment rectangular structure and several non-rectangular layout structures that utilize a distributed-channel dual-

drain device. Simulation results showed an improvement in worst case matching of at least two orders of magnitude over what is attainable with the standard two-segment common centroid layout scheme in the presence of linear threshold gradients. The four-segment dual-drain distributed-channel structures have similar matching characteristics to the four-segment rectangular structure but a better overall area budget. A comparison of the performance of several layout structures has shown substantial differences in the sensitivity of the mirror gain due to parameter gradients.

Acknowledgements

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CHAPTER 5. GENERAL CONCLUSION

Existing approaches for modeling matching performance in the presence of systematic and stochastic mismatches have shown considerable discrepancies between predicted results and actual measured performance. These discrepancies are inherently attributable to the use of the integral model. The error due to the use of the integral model has been investigated in this dissertation. The magnitude of the error is not significant for many low-end applications, but is significant for high-end applications. For systematic mismatch, this work has given an overall view on how the prediction of the matching performance of a layout can be skewed by the use of the integral model. For random mismatch, a new model for characterizing the effects of random variation of model parameters in MOS transistors has been introduced. This model overcomes the inconsistencies inherent in the integral model. The new model can be used to predict the matching performance of non-rectangular devices. It can also be used to extract the true area proportionality constants of a process. Determination of the true area proportionality constants will help researchers to explain some of the unexpected observations related to random mismatch measurements.

A simulation tool suitable for predicting the systematic mismatch in the presence of arbitrary parameter gradients and random mismatch at current mirrors for arbitrary shapes has been introduced. Comparison of experimental and simulation results showed good correlation. This tool can be efficiently used to develop layout topologies with improved matching characteristics. It has been used to uncover some fundamental limitations in the previously unquestioned relationship between random variations and gate area.

Several new current mirror layout techniques have been introduced that offer substantial improvements in matching characteristics over what is achievable with the simple, interdigitized and the two-segment common centroid structures in the presence of linear parameter gradients. The layout techniques include a four-segment rectangular structure and several non-rectangular layout structures that utilize a distributed-channel dual-drain device. Simulation results showed an improvement in worst case matching of at least two orders of magnitude over what is attainable with the standard two-segment common centroid layout scheme in the presence of linear threshold gradients. The four-segment dual-drain distributed-channel structures have matching characteristics that are similar to the four-segment rectangular structure but at a better overall area budget. A comparison of the performance of several layout structures has shown substantial differences in the sensitivity of the mirror gain due to parameter gradients.